International journal of Engineering Research-Online
A Peer Reviewed International Journal
Articles available onlne http://www.ijoer.in

Vol.1., Issue.2., 2013

RESEARCH ARTICLE

ISSN: 2321-7758

IMROVEMENT OF QUALITY OF POWER BY USING FUZZY LOGIC CONTROLLER OF DSTATCOM WITH REDUCED DC LINK VOLTAGE RATING FOR LOAD COMPENSATION UNDER NONSTIFF SOURCE CONDITION

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Article Received: 30/08/2013 | Article Revised on: 09/09/2013 | Article Accepted on:11/09/2013

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ABSTRACT— Due to the presence of nonlinear loads the quality of power have been distorted to improve the quality of power on of the shunt active filter have been introduced i.e. dstatcom. In dstatcom there will be mainly two topologies have been proposed they are proposed topology and hybrid topology. In the proposed topology of dstatcom will having the high average switching frequency and high switching losses and also THD present in the terminal voltages and source currents are high and also the voltage across the inductor will be high it causes the rate of rise of current and it causes the average switching frequency and average switching losses will be high so as to overcome these problems we can introducing the hybrid topology. In this project, hybrid topology for DSTATCOM applications with nonstiffsource is proposed. Non stiff source means the distribution substation can be taken as a remote area the distance between the remote area to load will be larger distance and large amount of feeder impedance will present the source will be known as nonstiff source. The hybrid topology enables DSTATCOM to have a reduced dc-link voltage without compromising the compensation capability they are proposed and hybrid topologies there will be mainly two capacitors have been used in hybrid topology. The two capacitors namely shunt and series capacitors. It uses a series capacitor along with the interfacing inductor and a shunt filter capacitor. With the reduction in dc-link voltage, the average switching frequency of the insulated gate bipolar transistor switches of the DSTATCOM is also reduced. Consequently, the switching losses in the inverter are reduced by using the shunt capacitor. Finally we can carried out the simulation study of proposed and hybrid topologies and also fuzzy logic controller of DSTATCOM. By using the fuzzy logic controller of dstatcom we can frother reducing the THD present in the source currents and terminal voltages.

Keywords

Dc-link voltage, distribution static compensator (DSTATCOM), Hysteresis current controller Conventional topology hybrid topology, nonstiff source, Average switching frequency, Reactive power.

INTRODUCTION

Due to the presence of power electronics devices, nonlinear loads, and unbalanced loads has degraded the power quality in the power distribution network [2]. To improve the quality of power shunt active filters have been proposed [3]-[5].The distribution static compensator (DSTATCOM) is a shunt active filter, which injects currents into the point of common coupling (PCC) (the common point where load, source, and DSTATCOM connected) such that the harmonic filtering, power factor correction, and load balancing can be achieved. In practice, the load is remote from the distribution substation and is associated with feeder impedance. In the presence of feeder impedance, the inverter switching's distorted both the PCC voltage and the source currents. In this situation, the source is termed as nonstiff. If the same control algorithm for the stiff sources is used for the nonstiff sources, the reference currents generated will be erroneous; the load compensation using state feedback control of DSTATCOM with shunt filter with shunt filter capacitor gives, however, better results [6]-[7]. The state feedback control of the shunt filter capacitor eliminates the switching frequency components in the terminal voltages and source currents. The compensation performance of any active filter depends on the voltage rating of dc-link capacitor [8]. In general; the dc-link voltage has much higher value than the peak value of the line-to-neutral voltages. This is done in order to ensure a proper compensation at the peak of the source voltage. In [9], the authors discuss the current distortion limit and loss of control limit, which states that the dc-link voltage should be greater than or equal to $\sqrt{6}$ times the phase voltage of the system for distortion-free compensation. When the dc-link voltage is less than this limit, there is insufficient resultant voltage to drive the currents through the inductances so as to track the reference currents. Reference value of the dc-bus capacitor voltage mainly depends upon the requirement of reactive power compensation of the active power filter [10]-[11].The primary condition for reactive power compensation is that the magnitude of reference dc-bus capacitor voltage should be higher than the peak of source voltage at the PCC [12]. Due to these criteria, many researchers have used a higher value of dc capacitor voltage based on their applications [13]-[18].

With the high value of dc link capacitor, the voltage source inverter (VSI) becomes bulky and the switches used in the VSI also need to be rated for higher value of voltage and current. This, in turn, increases the entire cost and size of the VSI. A few attempts have been made in the literature to reduce the dclink voltage storage capacity. In [19] and [20], a hybrid filter

has been discussed for motor drive applications. The filter is connected in parallel with diode rectifier and tuned at seventh harmonic frequency. Although an elegant work, the design is specific to the motor drive application and the reactive power compensation is not considered, which is an important aspect in DSTATCOM applications. In this paper, a new DSTATCOM topology with reduced dclink voltage is proposed. The topology consists of two capacitors: one is in series with the interfacing inductor of the active filter and the other is in shunt with the active filter.

CONVENTIONAL AND PROPOSED TOPOLOGIES OF DSTATCOM

In this section, the conventional and proposed topologies of the DSTATCOM are discussed in detail. Fig. 1 shows the power circuit of the neutral clamped VSI topology-based DSTATCOM which is considered the conventional topology in this study. Even though this topology requires two dc storage devices, each leg of the VSI can be controlled independently and tracking is smooth with less number of switches when compared to other VSI topologies. In this figure v_{sa} ,v_{sb} and v_{sc} are source voltages of phases a, b and *c*, respectively. Similarly, v_{ta} ,v_{tb} and v_{tc} are the terminal voltages at the PCC. The source currents in three phases are represented by i_{sa} , i_{sb} , and i_{sc} and load currents are represented by i_{la},i_{lb} and i_{lc}. The shunt active filter currents are denoted by i_{fa},i_{fb} and i_{fc} and *io* represents the current in the neutral leg. *Ls* and *Rs* represent the feeder inductance and resistance, respectively. The interfacing inductance and resistance are represented by *Lf* and *Rf* , respectively. The load constituted of both linear and nonlinear loads are as shown in this figure. The dc-

link capacitors and voltages across them represented by *C*dc1 = *C*dc2 = *C*dc and *V*dc1 = *V*dc2 = *V*dc, respectively. The current through the dc link is represented by the *i*dc. In this topology, the voltage across each dc-link capacitance is chosen as 1.6 times the peak value of the source voltages.

Fig. 2 shows the equivalent circuit of the proposed neutral clamped VSI topology-based DSTATCOM. It is a combination of the conventional DSTATCOM topology with a capacitor c_f in series with the interfacing shunt branch of the active filter and a capacitor *C*sh in shunt with the active filter. This topology is referred to as hybrid topology. The passive capacitor c_f has the capability to supply a part of the reactive power required by the load, and the active filter will compensate the balance reactive power and the harmonics present in the load. The addition of capacitor in series with the interfacing inductor of the conventional topology will significantly reduce the dc-link voltage requirement and consequently reduces the average switching frequency of the switches. This concept will be illustrated with analytic description in the following section. The shunt capacitor c_{sh} largely eliminates the switching frequency components of the VSI in the terminal voltages and source currents using state feedback control. The design of the series capacitor c_f and the shunt capacitor c_{sh} have significant effect on the performance of the compensator.

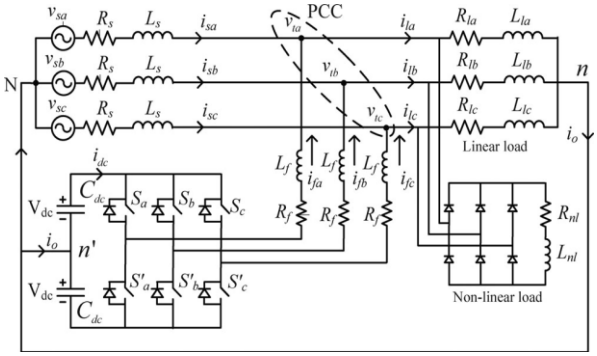

Fig. 1. Equivalent circuit of the neutral clamped VSI topology-based
DSTATCOM

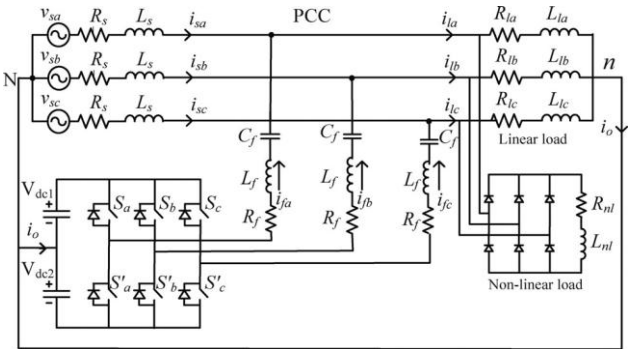

Fig. 2. Equivalent circuit of the proposed neutral clamped VSI topology-based DSTATCOM (hybrid filter)

II (A). Design of Shunt Capacitor Csh for the Proposed (or) hybrid VSI topology

In the presence of the feeder impedance, i.e., nonstiff source in the system, the terminal voltages are distorted due to unbalance and nonlinear load currents. Thus, these voltages as such can no longer be used to generate the reference quantities. In order to improve the performance, positive-sequence voltages at the terminal are extracted using the power-invariant instantaneous symmetrical transformation and are used for generating the reference currents. However, the terminal voltages are still contaminated with the inverter switching frequency components. These switching frequency components can be eliminated by providing a low impedance path using a filter capacitor Csh, connected in shunt at the PCC in each phase as shown in Fig. 2.While designing the shunt capacitor, it should be ensured that the feeder reactance *Ls* and the shunt capacitor Csh do not resonate at the fundamental frequency. If the filter capacitor resonates with the feeder reactance at a frequency ωr, then we get

$$c_{shr} = \frac{1}{w_r^2} \frac{1}{l_s} \quad (!)$$

When ωr is equal to fundamental frequency w_o the aforementioned capacitance is denoted as c_{sho}. Since resonance between the feeder reactance and shunt filter capacitor should be avoided at fundamental frequency, *C*sh should not be near to c_{sho}. If *C*sh is very large, the impedance between the PCC and ground becomes very small and results in high filter currents, which will, in turn, increase the source currents, so $c_{sh} >> c_{sho}$ is not valid. Thus,

*C*sh is chosen as 50 µF at 50 Hz as fundamental frequency for feeder impedance *Ls* = 0.01 H. A straightforward insertion of the shunt passive capacitor at the PCC may lead to stability issues and also with the increase in the capacitance value, the source currents and terminal voltages increase. The use of state feedback is one option to solve the problem, which is explained in the next section to simultaneously force the terminal voltage and the source current to be sinusoidal [24].

II (B). Design of Series Capacitor Cf for the Proposed (or) hybrid VSI topology

The fundamental filter current drawn by the shunt filter capacitor is neglected while designing the series capacitor value. This is because the impedance between the PCC and ground becomes very high when *C*sh is chosen much smaller than c_{sho} at fundamental frequency, and thus, the fundamental current drawn by the shunt capacitor is negligible. The design of the $c_f$depends upon the value to which the dc-link voltage is reduced. In general, loads with only nonlinear components of currents are very rare, and most of the electrical loads are combination of the linear inductive and nonlinear loads. Under these conditions, the proposed hybrid topology will work efficiently. The design of the value of c_f is carried out at the maximum load current, i.e., with the minimum load impedance to ensure that the designed will perform satisfactorily at all other loading conditions. If $s_{max}$is the maximum kVA rating of a system and v_{base} the base voltage of the system, then the minimum impedance in the system is given as

$$z_{\min} = \frac{vbase^2}{s_{max}} = r_l + j x_l \quad (2)$$

In order to achieve the unity power factor, the shunt filter current needs to supply the required load reactive current, i.e., the imaginary part of the filter current should be equal to the imaginary part of the load current. The filter current and load current in a particular phase are given as follows:

$$i_{filter} = \frac{v_{inv1} - v_{t1}}{r_f + j(x_{lf} - x_{cf})} \quad (2)$$

$$i_{load} = \frac{v_{t1}}{(r_f + j x_f)} \quad (3)$$

Where *V*inv1 and *Vt*1 are the line-to-neutral rms voltage of the inverter and the PCC voltage at the fundamental frequency, respectively. The fundamental component of inverter voltage in Terms of dc-link voltage is given as follows.

$$v_{inv1} = \frac{0.612\, v_{dc}}{\sqrt{3}} \quad (4)$$

DESIGN OF VSI PARAMETERS

The parameters of the VSI need to be designed carefully for better tracking performance. The most important parameters that need to be taken into consideration while designing conventional VSI are dc-link voltage v_{dc}dc storage capacitor c_{dc} Interfacing inductanceL_f, and switching frequencyf_{sw}. A detailed design procedure of VSI parameters is given in [23]; based on the following equations, the parameters of the conventional VSI topology are chosen.

The dc-link capacitor value is given by

$$c_{dc} = \frac{(2X - X/2)nT}{(1.8\, V_m^2) - (1.4 V_m^2)} \quad (5)$$

Where Vm is the peak value of the source voltage, *X* is the kVA rating of the system, *n* is the number of cycles, and *T* is the time period of each cycle. The interfacing inductance is given by

$$L_f = \frac{1.6 V_m}{4h f_{swmax}} \quad (6)$$

$$\text{Where} \quad h = \sqrt{\frac{K_1(2m^2-1)}{K_2\, 4m^2}}\, f_{swmax} \quad (7)$$

Where $k_1$and $k_2$are proportionality constants, fswmax is the maximum switching frequency of the switch, fswmin is minimum switching frequency of the switch, and *m* is given by

$$m = \frac{1}{\sqrt{1 - f_{swmin}/f_{swmax}}} \quad (8)$$

As mentioned earlier, the dc-link voltage reference (V_{dcref}) of the conventional VSI topology has been taken as 1.6 *Vm* for each capacitor [21], [22]. Consider a three-phase system with 230-V line-to-neutral voltage. The hysteresis band *h* is taken as 0.5 A. From (2), the interfacing inductance $L_f$is computed to be 26 mH. The base kVA rating of the system is taken as 15 kVA. Using (5), $c_{dc}$is computed and found to be 3300 µF. The system parameters are given in Table I for the conventional VSI topology.

IV. GENERATION OF REFERENCE COMPENSATOR CURRENTS UNDER UNBALANCED AND DISTORTED VOLTAGES

In this paper, the reference currents are generated using instantaneous symmetrical component theory [30] and are given as

$$i_{fa}^{*} = \frac{v_{ta}+\gamma(v_{tb}-v_{tc})}{\Delta}\left(p_{loss}+p_{avg}\right) \quad (9)$$

$$i_{fb}^{*} = \frac{v_{tb}+\gamma(v_{tc}-v_{ta})}{\Delta}\left(p_{loss}+p_{avg}\right) \quad (10)$$

$$i_{fc}^{*} = \frac{v_{tc}+\gamma(v_{ta}-v_{tb})}{\Delta}\left(p_{loss}+p_{avg}\right) \quad (11)$$

Where $\Delta = \sum_{j=a,b,c} v_{tj}^{2}$ (12)

$\gamma = \tan\varphi$ (13)

Here, p_{lavg} is the average load power, p_{loss} denotes the switching losses and ohmic losses in actual compensator and it is generated using a capacitor voltage PI controller. The term *P*lavg is obtained using a moving average filter of one cycle window of time *T* in seconds. The term $\phi$is the desired phase angle between the source voltage and current. In this paper, the load currents are unbalanced and distorted; these currents flow through the feeder impedance and make the voltage at PCC unbalanced and distorted. However, if the voltages are unbalanced and distorted, it is not possible to get balanced and sinusoidal currents after compensation. To remove this limitation of the algorithm, fundamental positive sequence voltages v_{ta}^{+} , v_{tb}^{+} , v_{tc}^{+} of the distorted terminal voltages are extracted. Now the voltages v_{ta},v_{tb},v_{tc} are replaced by v_{ta}^{+} , v_{tb}^{+} , v_{tc}^{+} now the expressions of the filter current equations are becomes

$$i_{fa}^{*} = i_{la} - i_{sa}^{*} = \frac{v_{ta}^{+}+\gamma(v_{tb}^{+}-v_{tc}^{+})}{\Delta^{+}}\left(p_{loss}+p_{avg}\right) \quad (14)$$

$$i_{fb}^{*} = i_{lb} - i_{sb}^{*}$$

$$= \frac{v_{tb}^{+}+\gamma(v_{tc}^{+}-v_{ta}^{+})}{\Delta^{+}}\left(p_{loss}+p_{avg}\right) \quad (15)$$

$$i_{fc}^{*} = i_{lc} - i_{sc}^{*}$$

$$= \frac{v_{tc}^{+}+\gamma(v_{ta}^{+}-v_{tb}^{+})}{\Delta^{+}}\left(p_{loss}+p_{avg}\right) \quad (16)$$

Where $\Delta^{+} = \sum_{j=a,b,c} v_{tj}^{2}$ (17)

$\gamma = \tan\varphi$ (18)

The aforementioned algorithm gives balanced source currents after compensation irrespective of unbalanced and distorted supply. The positive-sequence voltages that are extracted from the terminal voltages vta, vtb, and vtc are the reference filter capacitor voltages and are denoted by v_{sha}^{*} ,v_{shb}^{*} andv_{shc}^{*}. The reference filter capacitors currents are computed using these reference voltages and are given as follows:

$$\begin{matrix} i_{sha}^{*} \\ i_{shb}^{*} \\ i_{shc}^{*} \end{matrix} = \omega C_{sh} e^{j90} = \begin{matrix} v_{sha}^{*} \\ v_{shb}^{*} \\ v_{shc}^{*} \end{matrix} \quad (19)$$

Once the reference quantities *z*ref and the actual state vectors *z* are obtained from the measurements, the control signal for each phase is then computed using the reference and actual state vectors in the respective phases with the appropriate control gain *K*. The switching commands for the VSI switches are generated using the hysteresis band current control method. Hysteresis current controller schemes are based on a feedback loop, generally with two-level comparators.

Unlike the predictive controllers, the hysteresis controller has the advantage of peak-current-limiting capacity apart from in addition to other merits such as extremely good dynamic performance, simplicity in implementation, and independence from load parameter variations. The disadvantage with this hysteresis method is that the converter switching frequency is highly dependent on the ac voltage and varies with it. The switching signals generated for the VSI are as follows:

Uc = −K (z − zref)

u = hys (−K (z − zref)).

If h ≥ lim then hys (h) = −1, bottom switch is turned ON, whereas top switch is turned OFF (Sa = 0, s_a^{1}= 1).

If h ≤ lim then hys (h) = 1, top switch is turned ON, where as bottom switch is turned OFF (Sa = 1, s_a^{1}= 0).

The control circuitry is simple for both topologies because only three switching commands are to be generated. These three signals along with the complementary signals will control all the switches of the inverter.

V. SIMULATION RESULTS & TABLES

The same system parameters that are given Table I with *C*sh = 50 μF and *Cf* = 65 *μ*F are used in MATLAB simulation. The simulation results for both the

conventional topology and the proposed topology are presented in this section for better understanding and comparison between both the topologies. The load currents and terminal (PCC) voltages before compensation are shown in Fig 3 & 4. The load currents are unbalanced and distorted; the terminal voltages are also unbalanced and distorted because these load currents flow through the large amount of feeder impedance flowing in the system. Due to presence of nonlinear loads load currents will be unbalanced and distorted and also these will cause the source currents and terminal voltages will also unbalanced and distorted and will cause large amount of feeder impedance present in system.

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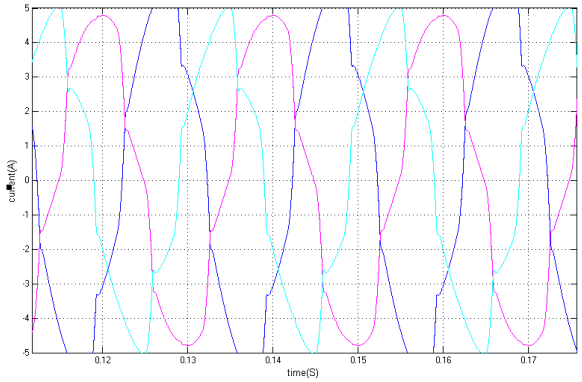
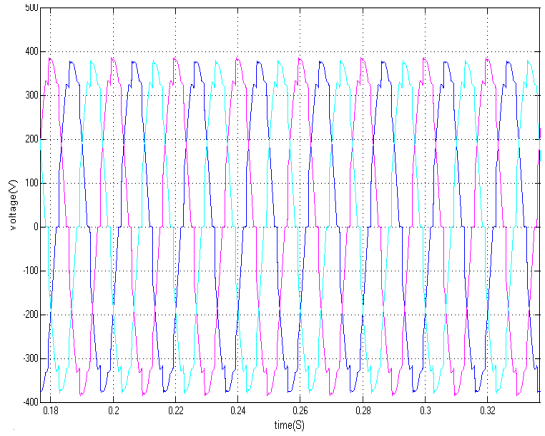


Fig.3.Load current waveform before compensation



F

ig.4 Terminal voltage waveform before compensation

Fig.5, 6, 7, 8, 9 gives the simulation results of the DSTATCOM using the conventional VSI topology. The source currents after compensation are balanced and sinusoidal as shown in Fig5. These currents still contain the switching frequency of the inverter. The dc-link voltages across the top and bottom dc-link capacitors are shown in Figs. 6, 7 using PI controller, the voltage across both capacitors are maintained constant to the reference value of 520 V as shown in the figure. The voltage across the interfacing inductor in phase-a is shown in Fig8. The peak-to-peak voltage across the inductor is 820 V. The terminal voltages contain the switching frequency components of the inverter and are shown in Fig9.

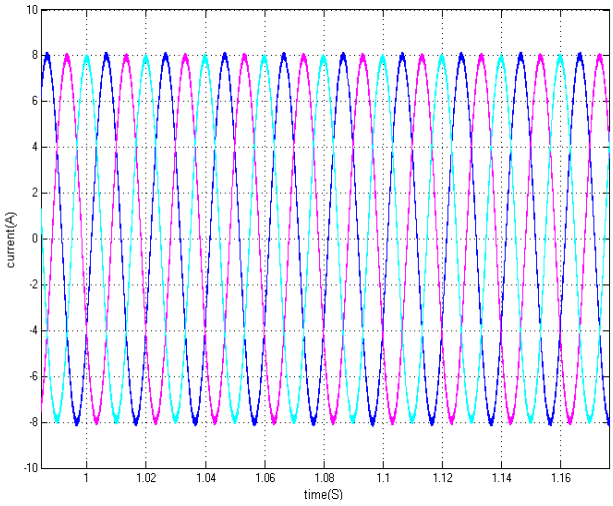


Fig5. Source currents after compensation in conventional topology of dstatcom

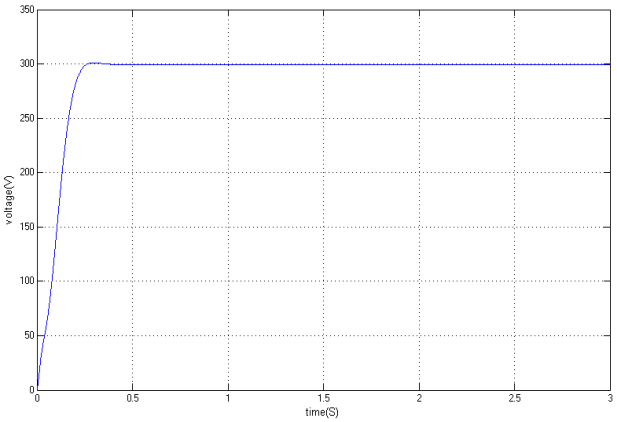


Fig6. Dc capacitor voltage waveforms at top side in conventional topology of dstatcom

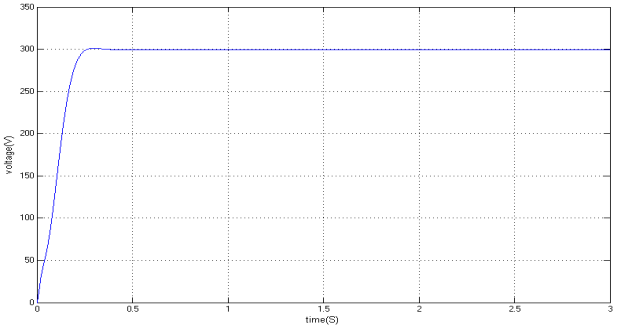


Fig7. Dc capacitor voltage waveforms at bottom side in conventional topology of dstatcom

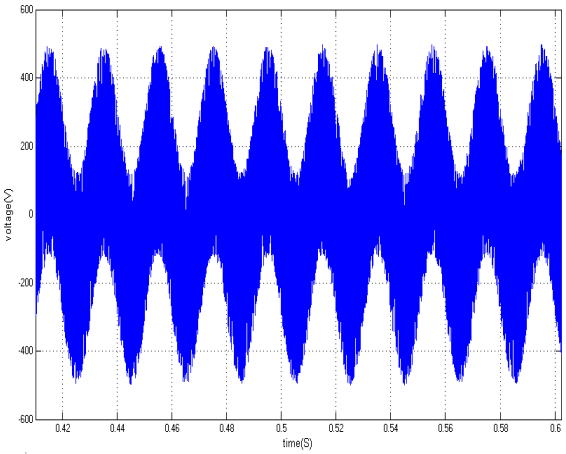


Fig8. Voltage across the inductor in phase-a in conventional topology of dstatcom

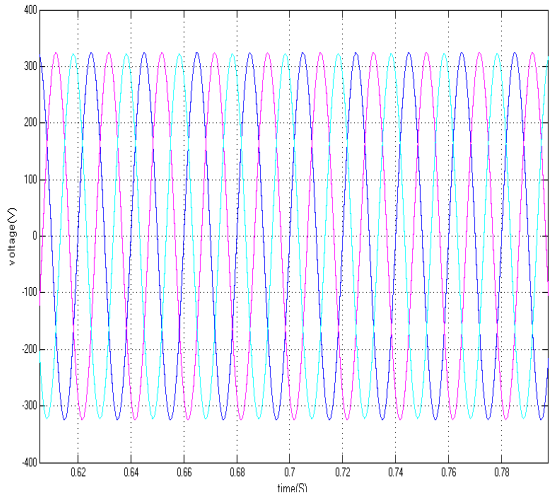


Fig9.Terminal voltages after compensation in conventional topology of dstatcom

Fig. 10, 11, 12, 13 gives the simulation results with the proposed (or) hybrid topology. The value of the capacitor Cf *in* the active filter branch is chosen to be 65 μF and the reference dc-link voltage is 300 V for each capacitor as discussed earlier. The shunt capacitor *C*sh is taken as 50 μF. The voltage across the capacitor in phase-*a* (vcf *a)* is shown in Fig.10&11. This figure also shows the phase-*a* terminal voltage vta and the voltage across the top dc storage capacitor *V*dc1. From the figure, it is clear that the voltage across the capacitor is in phase opposition to the terminal voltage. The reason beyond showing phase-*a* capacitor voltage is that the design of the reference dc-link voltage is based on phase-*a* filter current, which has the maximum filter current among the three phases. The source currents after compensation using proposed topology are shown in Fig.12. The compensator currents are displayed in Fig.5 which are identical to the currents using the conventional topology. The dc-link voltages across the top and bottom dc-link capacitors are

Shown in Fig10&11. The terminal voltage waveform after the compensation in hybrid topology is shown in fig.14. The voltage across the inductor is shown in Fig.13. The peak-to-peak voltage is 630 V, which is far lower than the voltage across the inductor using the conventional topology. As the voltage across the inductor is high in case of the conventional topology, the rate of rise of filter current dif /dt will be higher than that of the proposed topology. This will allow the filter current to hit the hysteresis boundaries at a faster rate and increases the switching, whereas in proposed hybrid topology, the number of switching does will be less. Thus, the average switching frequency of the switches in the proposed topology will be less as compared to the conventional topology.

Since the average switching is less, the switching loss will also decrease in the proposed topology. One more advantage of having less voltage across the inductor is that the hysteresis band violation will be less. This will improve the quality of compensation and total harmonic distortion (THD) will be less in the proposed topology. The terminal voltages after compensations in hybrid topology are shown in Fig.11, which are free from the switching frequency components of the inverter. The THD of the source currents and terminal voltages before and after compensation in all the three phases are given in table II and table III shows the THD of source currents and terminal voltages of hybrid dstatcom topology and fuzzy logic controller of dstatcom.

The following figs 15 &16 show the source currents and terminal voltages of fuzzy logic controller of dstatcom. From this we can observe that the THD present in the terminal voltage and the source current are further reduced when compared to hybrid topology of dstatcom. The voltage across the

inductor in phase-a as shown in fig17.From this we can observe that the rate of rise of current is to be less when compared to the hybrid topology of dstatcom. From this we can observe that the average switching losses will be less when compared to the hybrid topology of dstatcom. By using the fuzzy logic controller of dstatcom we can overcome the problems occurred in hybrid (or) proposed topology.

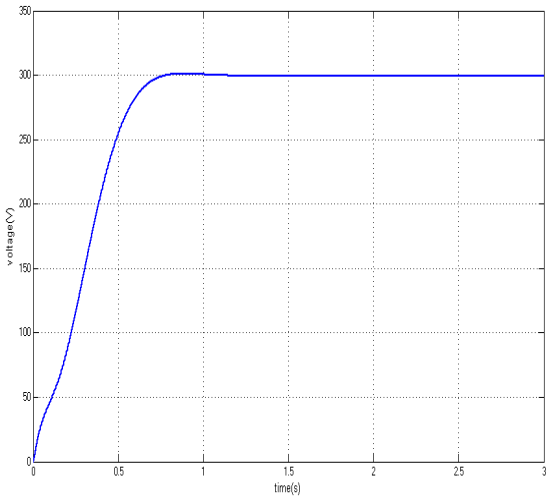


Fig10. Dc capacitor voltage waveform at bottom side in hybrid topology.

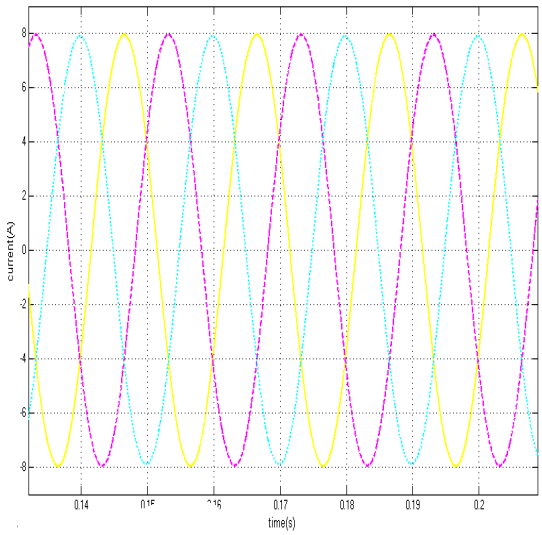


Fig11. Dc capacitor voltage waveform at lower side in hybrid topology.

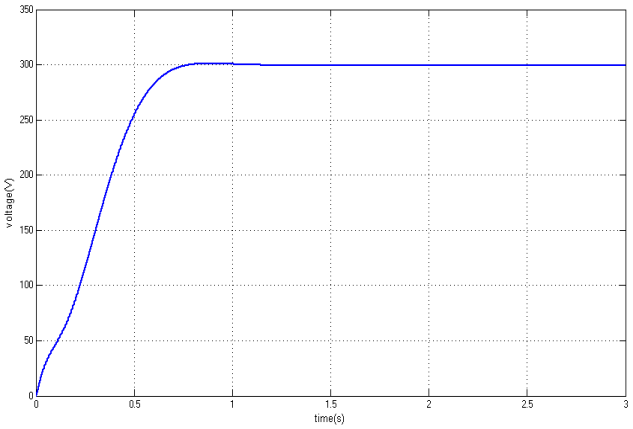


Fig12. Terminal current after the compensation in hybrid topology

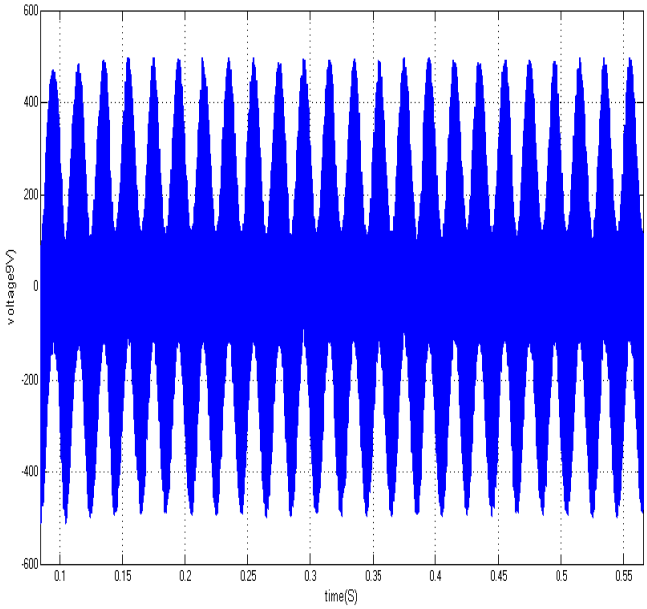


Fig13. Voltage across the inductor in phase-a in hybrid topology.

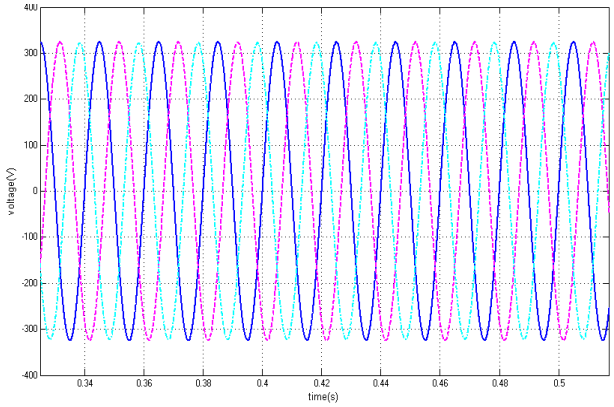


Fig14. Terminal voltage waveform after the compensation in hybrid topology.

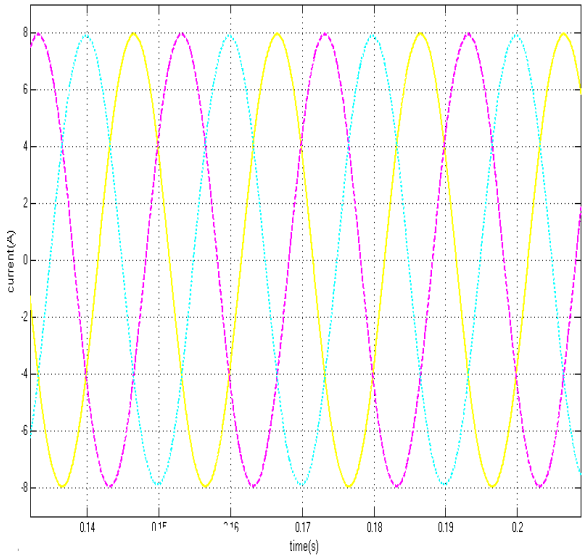


Fig15.Terminal voltage waveform of fuzzy logic controller of dstatcom

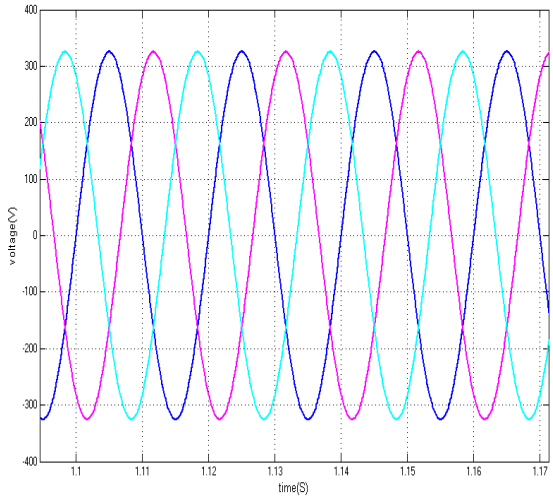


Fig16.Terminal current waveform of fuzzy logic controller of dstatcom

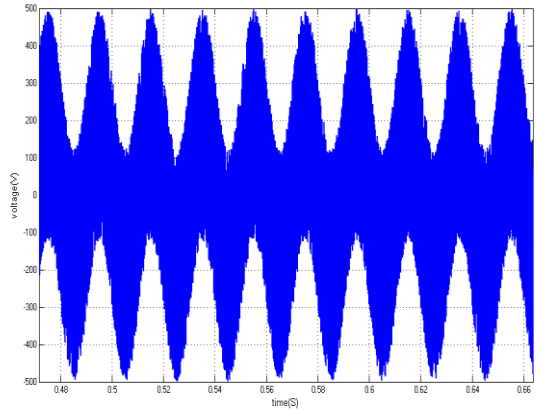


Fig17.The voltage across the inductor in phase-a of fuzzy logic controller of dstatcom

Table I : System parameters

System Quantities	Values
System voltages	230 V (line to neutral), 50 Hz
Feeder impedance	$Z_s = 1 + j3.141\ \Omega$
Linear load	$Z_{la} = 34 + j47.5\ \Omega$, $Z_{lb} = 81 + j39.6\ \Omega$, $Z_{lc} = 31.5 + j70.9\ \Omega$
Nonlinear load	Three phase full bridge rectifier load feeding a R-L load of 150 Ω-300 mH
VSI parameters	C_{dc}=3300 μF, V_{dcref}= 1.6V_m= 520 V, L_f= 26 mH, R_f= 0.1 Ω
PI controller gains	K_p=2, K_i=0.5
Hysteresis band (h)	± 0.5 A

TABLE II: THD OF SORCE CURRENTS AND TERMINAL VOLTAGES OF CONVENTIONAL AND HYBRID TOPOLOGY

THD (%)	CONVENTIONAL TOLOGY WITH DSTATCOM	HYBRID TOPOLOGY WITH DSTATCOM
i_{sa}	1.48	0.60
i_{sb}	1.60	0.69
i_{sc}	1.92	1.31
v_{sa}	3.5	0.24
v_{sb}	4.04	0.27
V_{sc}	3.49	0.93

TABLE III: THD OF SOURCE CURRENTS OF AND TERMINAL VOLTAGES

THD (%)	HYBRID TOLOGY WITH DSTATCOM	FUZZY LOGIC CONTROLLER WITH DSTATCOM
i_{sa}	0.60	0.00
i_{sb}	0.69	0.00
i_{sc}	1.31	0.00
v_{sa}	0.24	0.00
v_{sb}	0.27	0.00
V_{sc}	0.93	0.00

CONCLUSION

Finally we can concluded that the proposed (OR) hybrid topology has less average switching frequency, less THDs in the source currents and terminal voltages with reduced dc-link voltage as compared to conventional topology And also by using the Fuzzy logic controller with dstatcom we can reduce the THD in source currents and terminal voltages are further reduced as to compared to the hybrid (OR) proposed topology.

Acknowledgement

I am very thankful to Narasaraopet engineering college which provided me excellent lab facilities for completion of my project.

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