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RESEARCH ARTICLE

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Design of an 8-bit Successive Approximation Register Analog to Digital Converter using 0.18 µm CMOS Technology

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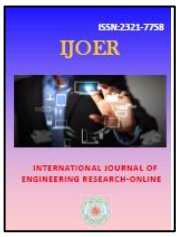

ABSTRACT

Mixed-Signal Design in today's industry is witnessing an increasing dominance by CMOS technology. With an increasing demand for miniature audio, video and other communication devices, the design of effective mixed-signal devices is becoming extremely critical. The design of a mixed-signal system is extremely complicated due to intricacies of analog design and the problems encountered in the integration of analog and digital sub-systems. The design process is best accomplished by transistor-level schematics and simulation. This can be attributed to the lack of fully developed modelling languages and automation tools in the realm of mixed-design. The aim of this research is to explore the possibility of a significant improvement in the sampling frequency of CMOS Successive Approximation Register ADCs (SAR ADC) based on binary search algorithm. The transistor level schematics of all the blocks are integrated to form a flat transistor level 8-bit SAR ADC circuit in 0.18 µm CMOS technology. The behaviour of each of these blocks and the integrated system has been verified with simulation in S-edit Tanner tool

Keywords— CMOS, Register ADC, S-edit Tanner tool, Analog signal, Digital Signal

I. INTRODUCTION

Analog to digital conversion is continuously ingredients in separate rooms; this many times in our daily lives. This conversion is made through an electronic apparatus which is recognized as analog to digital converter. ADCs have been proposed and utilized by demonstrating the electrical operations of Boolean algebra from Claude Elwood Shannon founded digital circuit design theory [1].

Now a day, every mixed-signal digital signal processing (DSP) arrangement by an analog input, such as audio and speech signal processors, sonar and radar signal processing systems, sensor arrays, wired/wireless communication systems, biomedical systems, seismic data processors, spectral estimation, etc., uses an ADC.

Successive Approximation Register A/D converters (SAR ADCs) [2] represent a substitute to pipelined ADCs and delta-sigma ADCs. As one of the commonly used Nyquist-rate ADCs, SAR ADCs are eminent for its better energy efficiency, little chip area, and more significantly, brilliant technology scalability.

In this work, 8-Bit ADC consecutive general register (SAR ADC) estimate. The main purpose is to reduce the power consumption of the micro-w. The proposed SAR ADC can be considered at the transistor level to 0.18 micron CMOS process. From this simulation, ADC reaches the entire energy use for micro 790.37w power supply.

II. RELATED WORK

C. E. Shannon et al [1] give the SAR employs a separate sequencer and registration code from the

D flip-flop. This design gives the benefit of simplicity and convenience in construction. It consists of the reproduction of each bit cells containing the two D-flip-flops.

Howard T Russell et al [2] give in the design of a single D flip flop is used in each bit cell phone which functions at the same time as the serial and registration code. This design is often referred to as a serial/code registered design. But the important point is to add a new section to the order to manage logical clock and data input into each cell.

Silvia Dondi et al [3] give the design consists of N=6 J-K flip flops which are utilized as code and shift register with the number of inputs as r given by comparator output. The single line result on the basis of JK-Flip flops fails to give the power consumption benefits. It uses the asynchronous feedback through the AND gates which has a tendency to limit the maximum clock frequency.

Yung-juichen et al [4] give the SAR is utilized for biomedical field and operates at a low supply voltage of one volt. A Boosted switch for the S/H stage, a split capacitor array for the D/A translator and the clocked rail to rail

comparator are supportive and are used to attain small power consumption. This design was realized with 0.18micro meter CMOS Technology.

Jens Sauerbrey ei al [5] give SAR is used here to work at ultra-small value of voltages. The circuit is made up in 0.18 micro meter CMOS technology. In this design charge redistribution law is used for conversion, the design of DAC is accomplished by using Binary weighted capacitors.

Siamakm Mortezapour et al [6] give the implementation of the SAR in 1.2 Micro meter CMOS process has demonstrated. It has a small voltage, high signal of a sample of swing and hold and D/A Converter recognized with inverting op-amp bias current structure which is added in the op-amp negative input terminal to the bias in the op-amp input common-mode voltage near the ground to reduce the supply voltage.

III. PROPOSED MODEL

In this part, the elements who build the topology of the 8-bit Successive Approximation Analog to Digital Converter are conversed. The diverse components are designed and/or chosen to optimize the speed and accuracy of converter.

Figure 1 exhibits the block diagram of the SAR ADC. It consists of a track and latch comparator, a digital logic block, an R-2R ladder DAC incorporating and a sample-and-hold circuit. The digital logic block includes a successive approximation register for binary search method which consists of D-Flip flop and a switching network to be executed at the bottom of R-2R ladder DAC.MOS resistors are employed in DAC which utilize small power in contrast to other resistors. Every block of ADC is designed in S-edit simulator with 0.18µm CMOS technology.

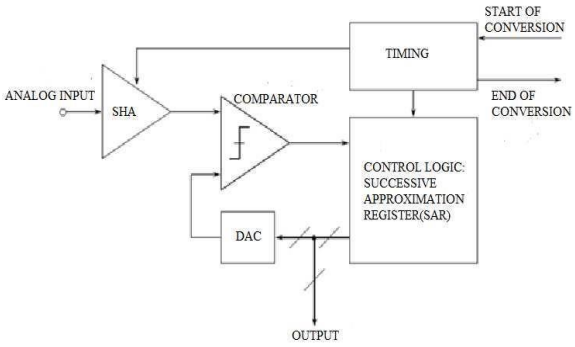

Figure 1 Block Diagram of SAR ADC

Sample and Hold Circuit: The requirements of the sample and hold circuit are that it should work consistently at high frequencies in the range of MHz. The time necessary to sample the analog input does not change the extent of each step in a translation phase. This is because the input is sampled previously and the identical value is applied as a reference during the time of translation. Though it is mandatory for each conversion, a fresh sample of the analog input is offered. This method of obtain a fresh sample should modestly change the translation period.

The schematic of sample and hold circuit is displayed in figure 2.Transistor M4 (NMOS and M15(PMOS) builds a transmission gate ,capacitor Co is the holding capacitor from which output is obtained. The clock is set as a control signal to the transmission gate and a sinusoidal signal is used as an input to the transmission gate. The sampled output is received across the capacitor.

Successive Approximation Registers: Successive Approximation Registers contains shift register and control registers. The shift register is made by using reset only D-Flip flops and the control registers is made by using set-reset D-Flip flops. The output of SAR is the final digital output of ADC.

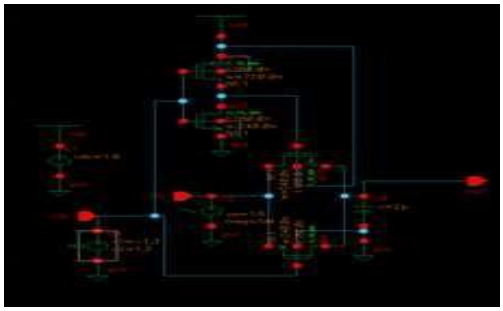

Figure 2 Schematic of Sample and Hold Circuit

SAR sustains three major actions: initially, it transfers the primary guess "1" to the right side through one bit; the second it takes the result from the comparator through positive triggering of the forthcoming bit; The third it saves the strong bits. After eight clocks, SAR displays the Pulse that means that one entire transfer process completed.

Table 1 The states in a Successive Approximation Register of an 8bit ADC

Conversion Step	Input Word								Comparator Output
1	1	0	0	0	0	0	0	0	d7
2	d7	1	0	0	0	0	0	0	d6
3	d7	d6	1	0	0	0	0	0	d5
4	d7	d6	d5	1	0	0	0	0	d4
5	d7	d6	d5	d4	1	0	0	0	d3
6	d7	d6	d5	d4	d3	1	0	0	d2
7	d7	d6	d5	d4	d3	d2	1	0	d1
8	d7	d6	d5	d4	d3	d2	d1	1	d0
Result	d7	d6	d5	d4	d3	d2	d1	d0	-

Thus the SAR can be enlightened as a FMS machine which will produce an estimate of consecutive steps or N states. From the general steps of m, where m = 1, 2 ...N, three probable events for a single bit N, probably causing the ' 1 ' using the selection of comparator or Holding bits per step (m-1).The cycle for N=8 is illustrated in TABLE 1.

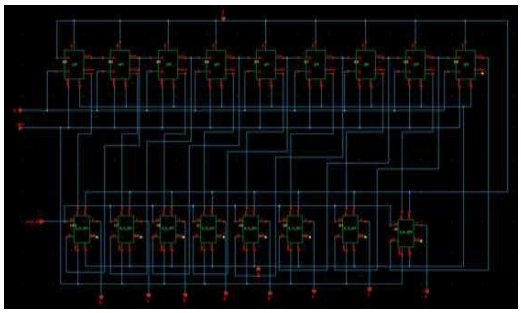

Figure 3 Schematic of Successive Approximation Register

8bit Successive Approximation Register ADC: On the establishment of the conversion cycle, a 'start' signal is created by the SAR control. This puts a starting pattern of "1000_0000" in the SAR. DAC produces analog values corresponding to the initial digital form. This value is computed adjacent to exit of the sample and hold circuit comparator. Based on this result MSB comparator changed to zero or one in the next step. This method completed for the MSB and it will repeat for total residual bits. Assessment of eight bits acquires nine clocks with the first step, which introduced starting in the template. The tenth cycle is generated as a result of all the eight bits and the latest digital output completion to be blocked. The graphic of an 8 bit ADC is revealed if figure 4. The R-2R ladder DAC is linked in the feedback (i.e. the digital output of successive approximation register is given to the input of DAC).

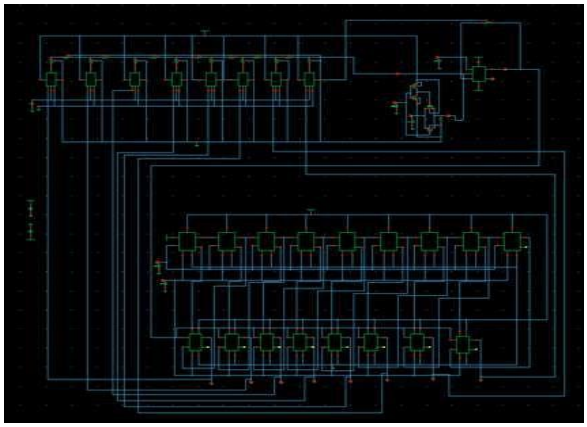

Figure 4 Schematic of 8 bit Successive Approximation Register ADC

Therefore, the ADC feedback mechanism is used to produce a digital code is analogous to an analog signal at its input. At each stage of the cycle of successive approximation conversion register must evaluate the digital code in such a way that the output of digital-to-analog converter tries to track the results of the sample and hold circuit as close as feasible. This was perhaps the result of the comparator at the latest every step that contributes to the SAR.

IV. EVALUATION AND EXPERIMENTAL

Simulation outcomes achieved by the design of the Successive Approximation Analog to Digital Converter are shown here. There are several models passed on each of the element. It is shown by the simulated waveforms of the ADC. Every part of the results is simulated in S-edit simulator.

a) **Sample and Hold Circuit:**Simulation outcome of Sample and Hold circuit is illustrated in figure 5. The input sinusoidal signal is sampled with the clock, whenever clock is high it follows the input

signal and when clock is low it keeps the value until the clock will become high another time.

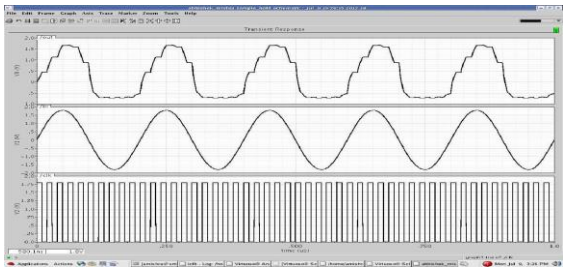

Figure 5 Waveform of Sample and Hold Circuit

b) **Track and Latch Comparator:**Simulation output of comparator is demonstrated in figure 6.Here V_{inp} is the input sinusoidal voltage V_{re} is the reference voltage. These two inputs of comparator are compared, V_{re} = 500mV whenever V_{inp} goes high than the V_{re} the output of comparator goes high and vice-versa. Normally reset is held low when comparator is working, when it goes high comparator will stop working and its output goes low.

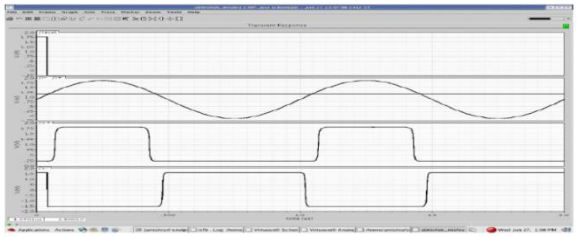

Figure 6 Waveform of Track and Latch Comparator

c) **Set-Reset Type D Flip-Flop**: Output of set-reset type D flip-flop is illustrated in figure 7. Generally it works when set and reset held high. Truth table is illustrated in table 2

Table 2 Truth Table of Set-Reset Type D Flip-Flop

S	R	Din	clk	Q	Qbar
HIGH	HIGH	HIGH	Z	HIGH	LOW
HIGH	HIGH	LOW	Z	LOW	HIGH
HIGH	LOW	X	X	LOW	HIGH
LOW	HIGH	X	X	HIGH	LOW
LOW	LOW	X	X		

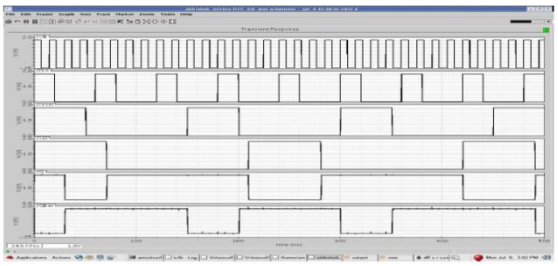

Figure 7 Waveform of Set-Reset Type D Flip-Flop

d) Successive Approximation Register: The successive approximation register consists of a shift register and its control logic to offer the last digital output. The outcome of an 8bit successive approximation register is illustrated in figure 8.

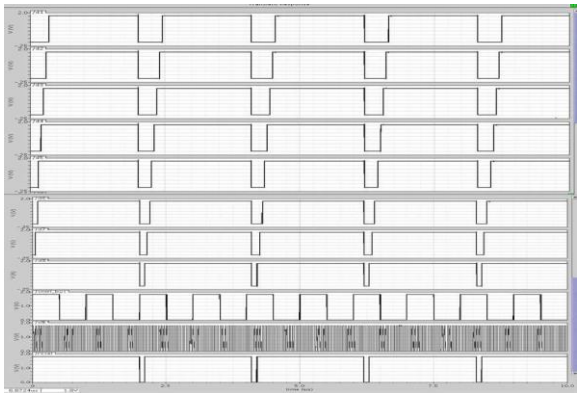

Figure 8 Waveform of 8bit Successive Approximation Register

e) Successive Approximation Register Analog to Digital Converter: Every block here is joined to build an 8bit SAR ADC. Outcome of an 8bit ADC is illustrated in figure 9

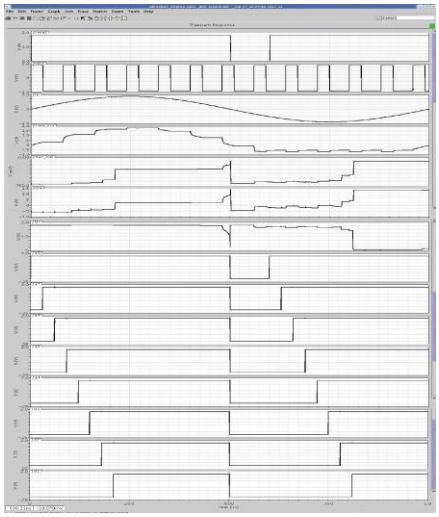

Figure 9 Transient waveform of an 8bit SAR ADC

Table 3 Results Summary

Parameter	Specification
Power Consumption	790.378µW
Supply voltage range	+1.8V to -1.8V
Reference	-10mV to 900 mV
Technology	0.18 micro meter
Highest Input frequency	1MHz
Resolution	8 bit
Output Noise	13.808 nV/Hz
Input Noise	10.409KV/HZ
Die Area	0.094609 mm^2

V. CONCLUSION AND FUTURE WORK

This part precisely gives the outcomes and the main research contributions of this work. Every blocks of 8bit SAR ADC has been generated (Schematic) and simulated with acceptable results. Entire schematics are simulated in S-edit Tanner tool under Analog Design environment.

The ADC assembled here is operated at 1MHz input frequency; the whole power utilization is 790.378 µW with 1.8 V power supply. The Layout of an 8bit ADC can form with die area of 0.094609 mm2 using 0.18 µm CMOS methodology.

Inside the comparator data transfer system is a substantial part all the time. In this system the translator depleted great efforts on the development of the comparator. The various topologies of comparator are examined. Track and latches the comparator is preferred for use by its low power. It produces more noise which weakens the input resolution and reduces the SNR.

This section describes the appropriate ADC in provisions less energy and fair solution and speed with the composition of the ADC available today.

Future work regarding this project includes the following:

1) Power dissipation can be condensed to some more amount by using C-2C capacitor array as a substitute of resistor array, Although it will raise the delay (i.e. diminish the speed) and die area of the design.
2) In this design effect of parasitic generated during RCX is not included, but in real application parasitic affects the linearity of ADC so there is a need to include these effects before fabrication of design. To reduce this parasitic, implementation of guard ring and shielding across the transistor is possible.
3) In this work perfect voltage reference source used during simulation. There are two approaches to the improvement of this situation- (i) Set up architectural diagrams and use as a reference voltage; (ii) Reference voltage circuit design with the sacrifice of extra power.
4) Implementation of BIST is also possible for testing of an ADC.

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