International Journal of Engineering Research-Online
A Peer Reviewed International Journal
Articles available online http://www.ijoer.in; editorijoer@gmail.com

Vol.5., Issue.1., 2017
January-February

RESEARCH ARTICLE

ISSN: 2321-7758

FPGA BASED MULTI RAIL CHOPPER BY USING MSP 430 PROCESSOR

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ABSTRACT

This paper proposed Mixed signal processor (MSP) based digital controllers are specifically optimized. The proposed Dual multiply¬-accumulate (MAC) architecture has implemented using field programmable gate array (FPGA) and design multi chopper. A detailed description of flexible Dual multiplier accumulator processor architecture is given and comparison is made with an existing solution with respect to application.

Keywords – Digital control, field programmable gate array, mixed signal processor (MSP), Programmable control logic

I. INTRODUCTION

The advantage of using mixed signal processors (MSPs) is a synthesizable 16 bit microcontroller. It is compatible with microcontroller family and can execute the code generated by a mixed signal processor 430 (MSPs) tool chain in a near cycle accurate way. The inherent flexibility of MSP mean it is can be programmed to execute different control laws. Multi-phase digital control has been achieved by means of field programmable gate arrays and fixed function ICs in recent implementation [1].

The MSP 430 processor comes with some peripherals they are, 16*16 hardware multiplier, watchdog, GPIO, Timer A, generic template. While being fully FPGA friendly, this design also particularly suited for ASIC implementation that is mixed signal ICs with strong area and low power requirements [3].

A mixed digital controller suitable for multi converters could also be used for controlling multiple independent converters, in each case multiple single cycle value must be calculated within single switching cycle [1]. Multiple converters are required in the powering of FPGA devices and other processor elements [1]-[2].

MSP 430 processor is one of the 16 bit RISC processor. The MSP 430 is a 16-bit microcontroller core compatible with MSP 430 family [3]. It is based on Von Neumann architecture, with a single address space for instructions and data. Only 16 bit data path only implemented. The processors mainly reduced the instruction and execution time and also reduce the cost and area. MSP are most suitable for wide

variety of multi rail applications [2], because they can be time multiplexed to execute multiple control algorithms and thereby control multiple power converters, as illustrated in Fig.1.

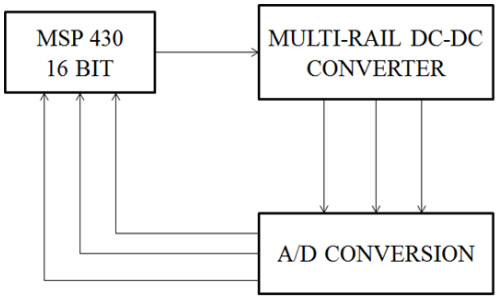

Fig.1. Mixed signal processor controlling multi rail dc-dc converter

It does also provide flexibility through their ability to be programmed to execute a different algorithm for each converter [1]. In addition to their computational features, general purpose MSPs usually contain other hardware that is required in the digitally controlled switching mode power supply system, for example, analog-to-digital converters and pulse width modulators [2].

II. PROPOSED PROCESSOR ARCHITECTURE

A. Overview

In this proposed topologies, MSP 430 processor based digital controllers are specifically optimized for multiple converters. The proposed Dual multiply-accumulate (DMAC) architecture has implemented using a FPGA and in a closed loop power converter system.

Fig.2.1 illustrates the proposed element has only Dual 16*16 bit data path only. The proposed main functional element contains program controller, register file etc. The program controller contains a finite state machine that determines the exact mode of operation and context of the processor. These elements are executing multiple algorithms in a time efficient manner.

The data path component effectively consist of single interconnected data path which receive data from a register file and share a number of functional elements, Data is transferred between the data path and the peripheral elements of the digital controller system through the data in and data out ports. Each of the interconnected data paths has a MAC unit to execute multiplication, addition, accumulate operations in a clock cycle. These operations are the main operations found in control algorithms [2].

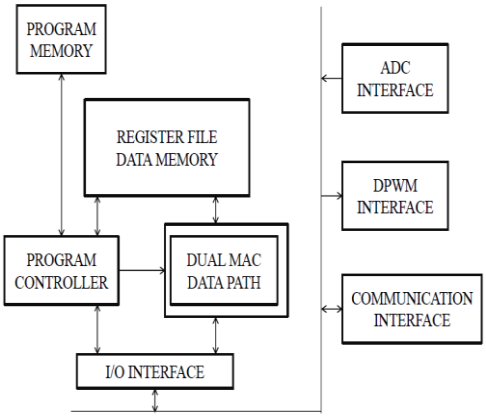

Fig.2. Proposed main functional elements.

B. Single MAC Data path

The data path component consists of Dual interconnected data path which receive data from a register file and share a number of functional elements, as illustrated in Fig.3. Data is transferred between the data path and the peripheral elements of the digital controller system through the data in and data out ports. The Dual data path has a MAC unit to execute multiplication, addition, subtraction operations in a clock cycle. Its operations are the main operations found in control algorithms.

The execution time of the control algorithms is therefore reduced by carrying out such operations. Data movement operation may also be executed in parallel with computational operation for filter delay lines. A Shifting and saturation operation means that more than one of these operations never needs to be executed simultaneously [2]. A barrel shifter and a saturator can therefore be shared between the Dual data path. The internal saturation logic limit the output of the accumulator register to prevent errors due to overflow. Other less frequently required functional elements are also shared the single data path, for example the Arithmetic Logic Unit (ALU), which can perform bitwise logical and, or, exclusive or, and inversion operations. The data path also includes a

separate limiter unit that can limit input, output, and register data values to any given threshold in a clock cycle operation. This facilitates limiting of the error from the analog to digital converter or limiting of the duty cycle that is applied to the digital pulse width modulator.

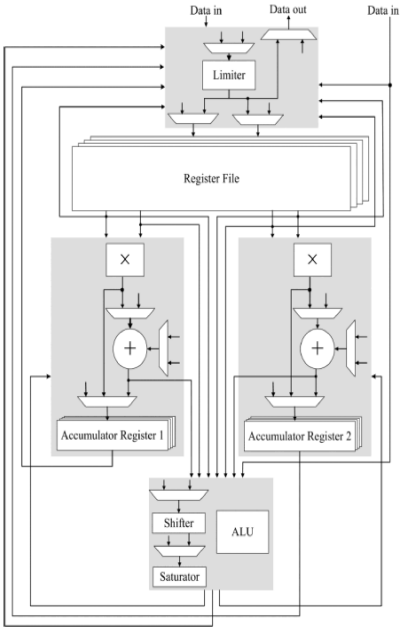

Fig.3. Proposed Dual MAC architecture

III. EXPERIMENTAL RESULTS

The processor was implemented using the Verilog hardware description language and synthesized using the integrated synthesizer in the FPGA design software from Modelsim and Xilinx ise, targeting implementation on a field programmable gate array (FPGA) device. The 16*16 bit multipliers in the data path of the processor were implemented using the embedded multipliers of the FPGA and the program memory was implemented using the embedded memory blocks. In order to maximize execution speed, the speed optimization synthesis option was selected. The synthesis process yielded a maximum achievable clock frequency due to the critical path from the register file memory, through the data path to the accumulator register. The multiplier and adder were found to be the main source of latency in the data path.

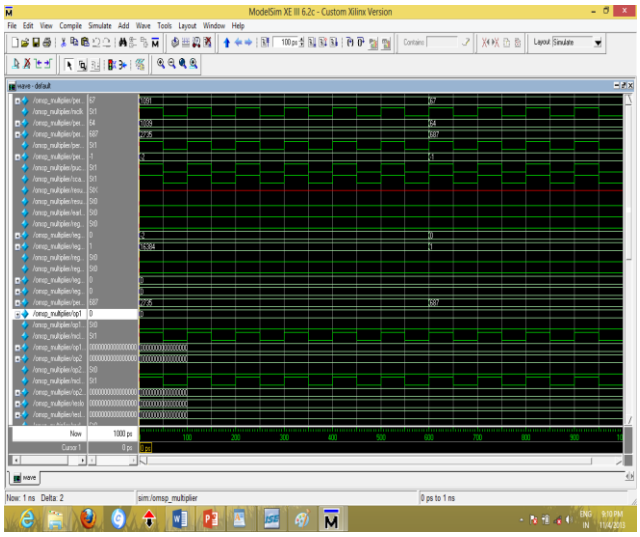

Fig.4. Simulation result of Dual multiplier accumulate

In the above Fig.4.The simulation output of hardware multiplier is obtained when the input of main system clock, peripheral inputs are given. Throughout the simulation the output patterns is matched with the given input.

TABLE I: PROCESSOR PERFORMANCE COMPARISON OF EXECUTION TIMES

	Proposed single MAC	Existing single MAC
Execution Time	350 ns	400 ns
Output Voltage	1.2 V	1.5 V
Number Of Bits	16*16 bit core	32 bit core

IV. SYNTHESIS REPORTS

The synthesis reports for the designed blocks are obtained. These reports show the clock and the timing information of each blocks designed.

Number of Slices: 110 out of 768 14%
Number of Slice Flip Flops: 71 out of 1536 4%
Number of 4 input LUTs: 195 out of 1536 12%
Number of bonded IOBs: 51 out of 97 52%
Number of MULT18X18s:1 out of 4 25%
Number of GCLKs: 1 out of 8 12%
Timing Summary:
Speed Grade: -5
Minimum period: 12.413ns (Maximum Frequency: 80.563MHz)
Minimum input arrival time before clock: 13.311ns

Maximum output required time after clock: 21.873ns

Maximum combinational path delay: 17.847ns

V. CONCLUSION

Processor consist of thirteen modules of which two modules are execution unit the other three modules are the memory backbone to the covered data and program memory and one module are frontend and one module belong to cpu and remaining six modules are peripherals. All modules are designed using Verilog coding and also simulated using the modelsim. The results that I had achieved are perfect as per the design description of the msp430 processor proposed.

VI. ACKNOWLDGEMENTS

My sincere thanks to Academic Dean Dr.P.Manimekalai and Assistant Professor Mr.M.Gowri Shankar for the helpful discussion and valuable suggestions about the presentation of this work.

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