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REVIEW ARTICLE

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REVIEW ON VARIOUS STRUCTURES OF 'VLSI' IMPLEMENTATION OF 'OFDM'

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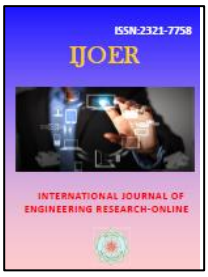

ABSTRACT

This paper concentrates on the review of Orthogonal Frequency Division Multiplexing (OFDM) technique, for digital data transmission and reception. OFDM is relied upon to be utilized as a part of future television and remote LAN (WLAN) systems. For instance, IEEE802.11 in the United States, ETSI BRAN in Europe [4], and ARIB MMAC in Japan have officially embraced the OFDM transmission technique as a physical layer for future broadband WLAN systems. In OFDM information transmission and reception uses IFFT and FFT in modulator and demodulator respectively. The literature review is carried from some of the journals.

Key Words—Discrete Fourier Transform (DFT), Fast Fourier Transform (FFT), Local Area Network (LAN), Orthogonal Frequency-Division Multiplexing (OFDM).

I. INTRODUCTION

OFDM is a unique instance of multicarrier transmission, where a single data stream is transmitted over various lower- rate subcarriers (SCs). It merits saying here that OFDM can be seen as either a modulation technique or a multiplexing technique. One of the principle motivations to utilize OFDM is to increase robustness against frequency selective fading or narrow band interference. In a single-carrier system, entire link can fail even if a single fade or interfere can occur, but in a multicarrier system, only a small percentage of the SCs will be affected. Error-correction coding can then be utilized to right for the couple of mistaken SCs [1]. With the fast development of advanced digital communication, there is the need for high- speed data transmission with faster rate. The mobile telecommunication industries are confronting the issue of providing the technology that be able to support a variety of services ranging from voice communication with a bit rate of couple of kbps to wireless multimedia in which bit rate up to 2 Mbps. Couple of frameworks have been proposed to determine the issue and OFDM framework has increased much consideration for distinctive reasons[2]. OFDM system was initially grown in the 1960s. Just lately, OFDM has been perceived as an exceptional strategy for high speed cellular data communication correspondence where its execution depends on very high speed digital signal processing applications. The strategy has just as of late get to be accessible with sensible costs versus execution performance of hardware implementation [3]. There are a few guaranteed focal points over OFDM with time-domain statistical multiplexing

- OFDM permits concurrent low-information rate transmission from a several clients.
- Pulsed carrier can be avoided.
- It reduces maximum transmission power for low data rate clients.

- Shorter and consistent delay.
- Contention- based multiple access (collision avoidance) is simplified. It, further improves OFDM robustness to fading and interference.

The remaining of this article is organized as follows after this introduction section, part II provides the previous literature on 802.11n standard OFDM system and its short description of literature. Finally part III provides the concluding remarks.

II. LITERATURE REVIEW FROM SOME SELECTED PAPERS

M. Merlyn et al. [4] focused on design and implementation of a variable-length prototype FFT/IFFT processor to cover various specifications of OFDM applications which is imple- mented on FPGA using Verilog HDL. He proposed a scheme for SDF (Single-path delay feedback) FFT architecture that employs a method of adding counter to achieve the purpose of programmable and without increasing the hardware complex- ity. The above proposed programmable SDF FFT processor can be applied to several OFDM communication systems. On the other hand, he also proposed a simple memory control method for shared-memory FFT architecture by acquiring the effective mixed-radix algorithm, and all of the calculation related to FFT will be discriminated in to three types: fixed- R-23, mixed-R-2 and R-23, and mixed-R-22 and R-23. The above two proposed methods of this paper can perform all FFT-point calculation in power of 2.

R. S. Brunda et. al. [5] designed a variable point FFT processor using FPGA to meet the requirements of OFDM sys- tem. They select 2D Fourier transform algorithm as the kernel algorithm. The detail design of two stage pipeline structure is presented using VHDL language, simulation is done on the Modelsim (SE) and verify on Spartan3E FPGA. The design can be utilized in real-time signal processing applications, which completes the principal computing modules in OFDM and OFDMA system.

H. Paul et. al. [6] OFDM is a bandwidth efficient signaling scheme for digital communications that was first proposed by Chang. The main difference between frequency division multiplexing (FDM) and OFDM is that in OFDM the spectrum of the individual carriers mutually overlap, giving therefore an optimum spectrum efficiency (asymptotically Q b/Hzformodulation of each carrier). OFDM carriers exhibit the prop- erty of orthogonality on a symbol interval if synthesized such that they are spaced in frequency exactly at the reciprocal of the symbol interval. There are two deleterious effects caused by frequency offset, out of which one is the reduction of signal amplitude in the output of the filters matched to each of the carriers and the second is introduction of ICI from the other carriers which are now no longer orthogonal to the filter. Because, in OFDM, the carriers inherently closely spaced in frequency compared to the channel bandwidth requirement, the tolerable frequency offset becomes very small fraction of the channel bandwidth requirement. Maintaining sufficient open loop frequency accuracy can become difficult with links, such as satellite links with multiple frequency channels estimations and translations or, as mentioned previously, in mobile digital links that may also introduce significant Doppler shift.

Dr. Nataraj et. al. [7] OFDM Kernel which advert to the inverse fast Fourier transform and cyclic prefix insertion blocks in the downlink flow and the FFT and cyclic prefix removal blocks in the uplink flow. An elongation to the OFDM kernel is required to affirm orthogonal frequency-division multiple access (OFDMA) that permits each user to be allocated with a portion of the available carriers. This technique is referred to as sub channelization and channel division. In this paper an additional controller is required for the cyclic prefix addition block that buffers the output packets from the FFT, which adds the appropriate proportion of the end of the output packet to the beginning of the output packet. A moderately significant memory resource is required; the hardware architecture has been designed so that the embedded memory may be shared with the uplink OFDM kernel if the modem is operating in time division duplex (TDD) mode.

D. Revanna et. al. [8] A Scalable FFT Processor Architecture for OFDM Based Communication Systems, in this paper radix-2 algorithm is used for FFT implementation. Also they proposed pipeline architecture. Pipeline architecture is also known as cascaded FFT architecture in which each stage has

its own processing element. The proposed architecture operates at fixed and variable length FFT processor and gives good speed, flexibility and scalability. It supports any N- point FFT. Author proposed from 16-point to 2048-point. It meets the requirement of various wireless standards. ROM is used for the storage of twiddle factors. It is found that clock cycles required for 64- point FFT processor are 254. The time required for the computation of processor is 1.27s. Also power required is 423.46mW.

M. Arioua et. al. [9] VHDL Implementation of an Optimized 8-point FFT/IFFT processor in Pipeline Architecture for OFDM systems, in this paper a 8-point FFT processor is proposed using Radix-2 algorithm with R2MDC (Radix-2 multipath delay commutator) architecture. Here two methods are used to reduce the number of complex multiplications. In first method, the implemented algorithm for complex multiplication uses three multiplications, one addition and two subtraction and in second method add and shift operation is used for the reduction of complex multiplications. From the results it is observed that no. of complex multiplications required for first method=4 and for second method=0. Henceit achieves the target of less resource usage.

N Kirubanandasarathy et. al. [10] VLSI Design of Mixed radix FFT Processor for MIMO OFDM in wireless Com- munications, in this paper author implemented 64-point FFT processor using mixed radix algorithm having combination of Radix-2 as shown in figure 1 and Radix-4. Here bit reversal architecture is used for implementing FFT processor. It is done for multi input multi output (MIMO) OFDM system. Hence it meets the requirement of IEEE 802.11n WLAN standard. The proposed paper reduces the hardware complexity and hence power gets reduced as it is using mixed radix algorithm. It requires no. Of CLB slices=750 Utilization factor=9.77% and power=3831.63mW.

Figure 1: Basic Butterfly Unit of Radix-2.

C. Shashikanth et. al. [11] This paper deals with the design and implementation of Fast Fourier Transform (FFT) algo- rithm which can be used for wireless-communication and its applications in real time environment. The computational strategy is two dimensional and implementation of this strategy on VIRTEX 5 LX330 FF1145 based XILINXs FPGA. The algorithm is written in VHDL language, which is verified and simulated on MODEL SIM SE tool, this provides new methodology to design and develop the processor for the Digital Signal processing prospects, and is implemented on the fundamental of pipelined architecture and Fast Fourier Transform approach.

K. Yang et. al. [12] Presents a multipath delay com-mutator (MDC)-based architecture and memory scheduling to implement fast Fourier transform (FFT) processors for multiple input multiple output-orthogonal frequency division multiplexing (MIMO-OFDM) systems with variable length. Based on the above architecture, they propose to utilize radix-Ns butterflies at each stage, where Ns are the number of data streams, so that there is simply one butterfly demand in each stage. Due to the simple control mechanism of the MDC, they propose simple memory scheduling scheme for input data and output bit/set-reversing. To apply the proposed method in practical applications, they use Ns = 4 and implement a 4-stream FFT/IFFT processor with variable length including 128, 512, 1024 and 2048 for MIMO-OFDM systems.

K. Harikrishna et al. [13] they presented a high level implementation of a high performance FFT for OFDM Modulator and Demodulator. The Verilog HDL coding is used for design and targeted into Xilinx Spartan3 FPGAs (a family of FPGA technology). They proposed a Radix-22 Algorithm and used it for the OFDM communication system. In proposed algorithm it has been examined that it uses the similar multiplicative complexity as the radix-4 algorithm, and it retains the butterfly structure of radix-2 algorithm.

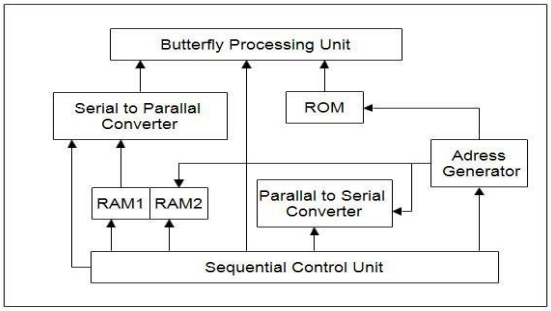

Figure 2: Block diagram of FFT processor.

Chandrakanth V. et. al. [14] Presented a simple and novel architecture for executing hardware effective real time config- urable variable point FFT implementation. This architecture is of generic in nature and its application can be elongated beyond radars. It can also use on custom designed FFTs in contrast to their usage of Altera IP core as shown in figure

2. But first the obtained data from the receiver has to be reorganized from range cell wise to Pulse repetition Interval (PRI) wise before providing as input to the FFT block, which is done with the help of ping pong memory architecture.

III. CONCLUSION

This research paper is a literature survey carried out in the FFT and its application in OFDM system. The paper presents the authors contributions towards the implementation of FFT and its applications in Wifi, Wimax and wireless communication systems. OFDM is especially suitable for high- speed communication due to its resistance to ISI. As communication systems increase their information transfer speed, the time for each transmission necessarily becomes shorter. Since the delay time caused by multipath remains constant, ISI becomes a limitation in high-data-rate communication. The implementation of FFT logic and Transceiver can be a great research for OFDM and OFDMA and multiple input multiple output (MIMO) OFDM systems.

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