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RESEARCH ARTICLE

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# DESIGN EXPLORATION OF AN I²C INTERFACE FOR TEMPERATURE SENSOR AND AN 'EEPROM' MEMORY USING 'VHDL'

**P.JEGADEESHWARI[1], D. KANIMOZHI[2], B. THEEBAN CHAKKARAVARTHY[3], A. NIVETHA[4]**

[1-4]Assistant Professor, CK College of Engineering and Technology

jegadeeshwari25@gmail.com, kanimozhi.gk@gmail.com; theeban_b@yahoo.co.in;nivethaadhi@gmail.com,


**ABSTRACT**

This paper is mainly based on I2C bus controller which communicates or interface between both master and slave devices i.e. FPGA and temperature sensor (SE95), EEPROM memory (24C02) and SSD display for serial communication. The implementing I2C bus on Field Programmable Gate Array is simpler when compared to others because it requires only two wires and less number of connections pins. Thus in our paper we are going to design and implement I2C bus using VHDL code which interfaces FPGA board and with temperature sensor with EEPROM memory and displayed on application circuit ie SSD display and synthesized using Xilinx 13.1 platform.

Key Words : I2Cbus, Master, Slave, VHDL, EEPROM (24C0) Temperature Sensor(SE95), Xilinx, FPGA- Field programmable gate array., SDA –Serial data line., SCL – Serial clock line.,TWI –Two wire interface .,I2C- Interconnect integrated circuit



## INTRODUCTION

Communication on PCB board is achieved by using number of buses, here we are introducing I2C bus which was introduced in the year 1980 by Philip's company. The main reason for using this was to reduce the connection between IC's. because it utilizes two bus line signals ie SDA (serial data line) and SCL (serial clock line). By nature SDA is bidirectional and SCL is unidirectional. I2C (interconnect integrated circuit) or TWI (Two wire interface) bus is synchronous 8 bit oriented serial communication bus. I2C bus interfaces main processor and as many peripheral devices and it consists of more than one master and can have as many slaves devices such as ADC, Memory, Oscillator etc. Each devices on I2C bus have unique addresses and this address consists of 7 bit or 10 bit. In this paper we are interfacing FPGA board with Temperature sensor and the temperature sensed data can be stored in EEPROM memory and it can be displayed on SSD display.

## I²C BUS PROTOCAL

### A. I2C Specification

I2C is synchronous 8 bit oriented serial communication bus, which consists of two signal lines and one common ground. The two wires are SCL and SDA , by nature SCL is unidirectional and SDA is bidirectional, both lines are used in order to transfer the data along with the clock signal. I2C bus consists of two or more number of masters and have as many as slaves. The number of slave devices connected onto the I2C bus it is addressed by different address where address consists of 7 bit or 10 bit and can transfer any length of data .There is acknowledgment bit sent by slave to master or vice versa, to ensure the data is received after each

data transfer. And it has four standardized speed modes, called standard (100 kbps), fast (400 kbps), fast- plus(1 Mbps) and high-speed(3.3 Mbps).

**B. DATA TRANSFER**

The data on SDA line it is stable when SCL line is high and when SCL line is low data can be exchanged. The data which is transferred on SDA line begins with START bit and ends with STOP bit. START operation happens when SCL line is high and SDA line is at falling edge (ie from high to low) and STOP operation happens when SCL line is high and SDA line is at rising edge (ie from low to high). Once this START operation begins bus is considered to be busy, bus becomes free once STOP condition appears. This is followed by 8 bit of device address here the 8th bit is considered to be read/write. If this bit is low than it is considered to perform write operation or else read operation. This is followed by ACK signal (acknowledgement signal), which indicates that operation is successfully completed.

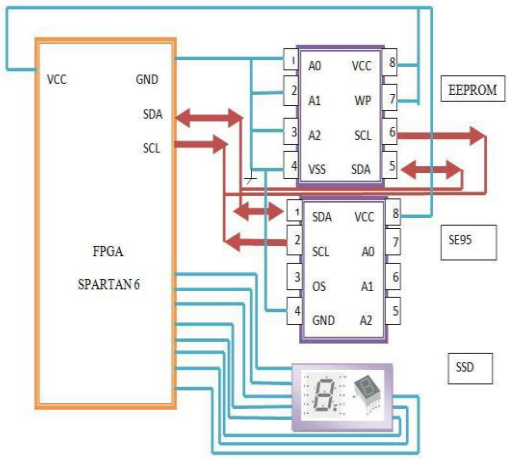
**C. Case of Multiple Master situation**

In this a problem arises -synchronization issue. Therefore, devices are connected in such a way that they are connected as a wired –AND conditions. The open drain /open collector characteristics of the FETs/Transistors/Gates in Wired –AND used as the devices to control the data collision of two masters. This is obtained by Arbitration techniques. That is when one master is transmitting a High level signal, while the other is transmitting a low level signal on the SDA line, the high level signal is allowed & the Low level signal is switched off. The reason being the SDA data must be in synchronous with the SCL while it is in High level. This is one way of arbitration. Another way, is that when two masters are trying to address the same device arbitration continues with the comparison of the data- bits to check the whether they are master –transmitter or acknowledge –bits if they are master-receiver. So the address and data is not lost during this arbitration process as it is determined by the winning master. A master that loses the arbitration can generate clock pulses until the end of the byte in which it loses the arbitration. If a master also incorporates a slave function and it loses arbitration during the address stage, it's possible that the winning master is trying address it. Then the losing master should switch over to slave mode. However, the arbitration is not allowed in repeated start & data, a stop condition & data and a repeated start & stop condition. Also the slave is not allowed in the arbitration procedure.

**PROPOSED SYSTEM**

The design of this project consists of FPGA board which is interfaced with EPROM memory and temperature sensor and the temperature sensor sense the value and those value will be written into EPROM memory and it can be displayed on application circuit ie SSD display. This temperature sensor can be used in industry or in ovens etc in order to sense the.

temperature and indicate the value of the temperature The interfacing is done using I2C bus protocol which consists two line SCL and SDA these two lines are connected to power supply using pull up resistor and these resistor values depends on number of slave devices connected to master. So if the number of slave device increases the resistor value decreases.

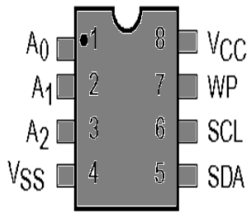



**IMPLMENTATION OF I2C FOR EEPROM MEMORY (24C02)**

EEPROM memory it is 256 byte ie 2k bit with 32pages each page consists of 8 byte.

**A. FEATURES**

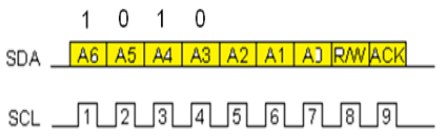
- Low-voltage and standard-voltage operation -1.8(Vcc = 1.8V to5.5V).
- Internally Organized 128x8 (1K), 256x8 (2K), 512x8(4K), 1024x8(8K)or 2048x8 (16K).
- Two-wire serial interface
- Write protect pin for hardware data protection




| Pin Name | Function |
|---|---|
| A0, A1, A2 | Device Address Inputs |
| SDA | Serial Data/Address |
| SCL | Serial Clock |
| WP | Write Protect |
| $V_{CC}$ | +1.8V to +6V Power Supply |
| $V_{SS}$ | Ground |

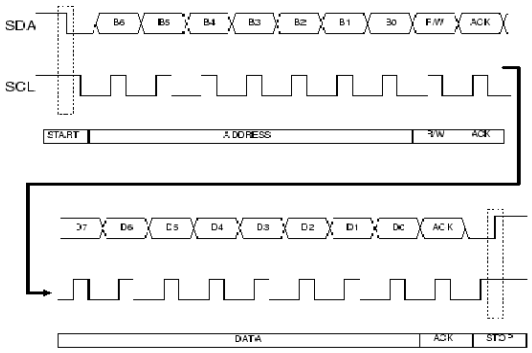
**DEVICE ADDRESSING OF EEPROM MEMORY**

The addresses of all I2c bus are either 7 bits or 10 bits. The modules and all the common chips which we connect to I2c bus will have 7 bit address. This means that I2C bus can have up to 128 devices, since 7 bit number can be from 0 to 127. We always send 8 bit address , the extra bit is used to inform the slave if master is writing to it or reading from it, if bit is zero the master is writing to clave device. If bit is 1 then the master is reading from slave. For an EEPROM(24C02) device the 4 MSB's are fixed as "1010", the rest 3 bits ie A0 A1 and A2 are programmable, so we cannot maximum of 8 EEPROM(24C02) devices Figure shown below gives the clear idea of addressing byte. During transmission of data bits in I2C it transmit from MSB to LSB during implementation using VHDL.




**Writing Data to EEPROM (24C02) Device**

1. Send a start sequence
2. Send the I2C address of the slave with R/W bit low (even address)
3. Send the internal register number in which you want to write to
4. Send the data byte
5. Optionally send any further data bytes.
6. Send the stop sequence.




**Reading Data from EEPROM(24C02) Device**

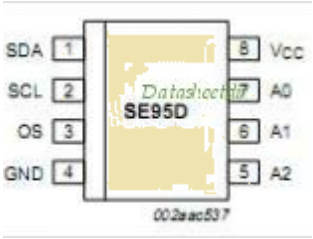
- Send a start sequence.
- Send 0xC0 (I2C address of the device with R/W bit low(even address).
- Send 0x01 (Any Internal address of the bearing register).
- Send a Start sequence again.
- Send 0xC1 (I2C address of the device with the R/W bit high (odd addresss).
- Read data byte from device
- Send the stop sequence.

**TEMPERATURE SENSOR (SE95)**

***General description***

SE95 is a temperature sensor which converts temperature value into digital values by making use of an on-chip band gap temperature sensor with sigma delta analog-to-digital conversion techniques. And this device also consists thermal detector which detect over temperature and provides output. And by using controller via the 2 wire serial i2c bus interface can access the data registers contained in SE95. When temperature exceeds, an open-drain output (pin OS) which includes in device becomes active. And it consists three selectable logic address pins ie A0. A1, A2, so that bus can connect eight devices without address conflict.

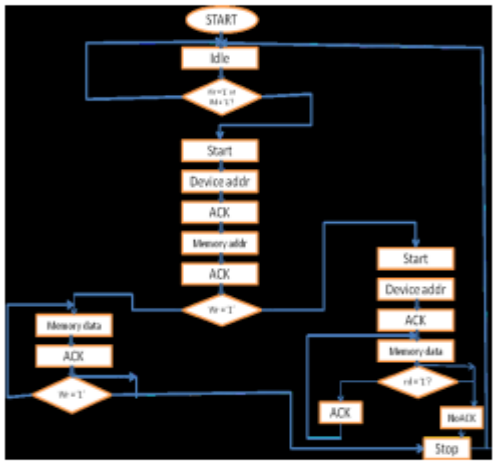
**PIN CONFIGURATION OF SE95**

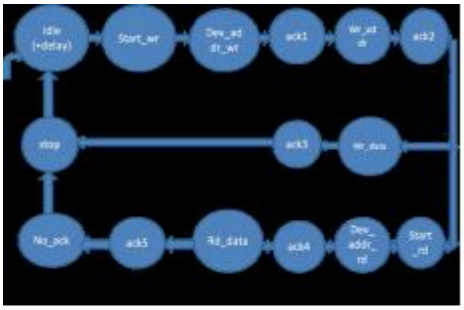


**FEATURE**

1. Temperature range from -55 °C to +125°C.
2. I2C-bus interface to 400kHz with 8 devices on the same bus
3. 13-bit ADC that offers a temperature resolution of 0.03125 °C.

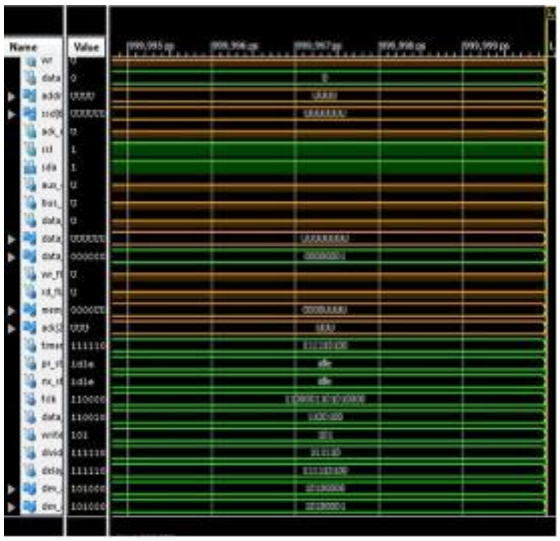
**FLOWCHART:**



**IMPLEMENTATION RESULT**

I2C bus protocol is designed and implemented in VHDL using 13.1 Xilinx platform. The device waveform and device utilization summary is given below



**CONCLUSION**

In this Paper, we have more particularly focused on design features and utilization issues of high-quality I2C Master/Slave IPs based upon design-reuse methodology. The design process is simplified using VHDL and here 3 slaves been connected, this I2C protocol can handle as many number of slaves which helps in PCB or single board in order to connect as many peripheral devices. Therefore this protocol can be used in real time system where data cannot be lost and the design is simple because it makes use of two wires.

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