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FPGA BASED DESIGN AND SIMULATION OF EXTENDED GOLAY CODEC WITH DELAY OPTIMIZATION FOR HIGH SPEED APPLICATIONS

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ABSTRACT

In wireless communication world the topic which matters a lot is error detection capability of the receiver that is very most issue to be considered for communication. The ability of the receiver to detect the errors and correct them from the received information is achieved with the help of error correction codes (ECC), so as to provide correct information data to the processor. A number of different error correction codes are available to implement the hardware and software with such preference. But, when the length of the communication link becomes very long, i.e., the distance between the wireless transmitter and receiver is very large, the effect of noise on the transmitted signal may cause a change in multiple bits of the transmitted information. This can cause drastic loss in many cases. In this brief a Field Programmable Gate Array (FPGA) based design and simulation of Golay Code (G23) and Extended Golay Code (G24) Encoding scheme are presented. This work is based on the optimization of the time delay of the operational circuit to encode a data packet using the Golay Encoder.

I. INTRODUCTION

The Technique which is used for re retrieving of the information is called Hashing and one of the major factor of this technique that it requires a linear time of complexity in most cases. One of the most important key features of the hash searching techniques is the hash function. These key features are basically used in order to achieve the required performance, simplicity and storage reduction. In this technique simple mathematical functions are used like modulus. This paper presents a new function which is to be used for searching techniques. This mathematical functions function depends on the decode operation of the famous Golay code (24, 12, 8) error detection and correction technique, which would also expressed or named as extended Golay code. This paper mainly focused on the performance characteristics along with the explored capabilities of the proposed design. A technique which is widely used in information retrieval, in the condition when the search key is known and same as that of the stored in the senders memory this technique is called hash technique. On the other hand, approximate matching algorithms should be implemented to handle the situation when only partial information of the object is available.

This paper presents a brief description about the work done to implement the results on application of golay and plan to work on Extended golay code to implement it on FPGA for a new technique which overcome the drawback of

previous work and present better result, in which we define a new function that is based on the decode operation of Golay code (24, 12, 8).

II. GOLAY CODE

GOLAY code technique based encoder and decoder using CRC methodology. This work is to increase the secure level and to optimize the circuit complexity. Golay system is used to modify the encoder and decoder data bits structure level and to add the message bit, key bit and to apply the these bits into GOLAY binary code technique. This technique is to apply the majority gate analysis process and to get the final majority output bit and to add the any location in encoder architecture output data bits. To fight this problem, a hardware module programmed to yield a Golay encoded codeword may be used. Golay decoder is used extensively in communication links for forward error correction. Therefore, a high speed and high throughput hardware for decoder could be useful in communication links for forward error correction. Literature surveys were conducted, which deal with encoding methods for Golay code, but these are not suitable for hardware implementation due to complexity the algorithms. The equations are then used to implement a data flow representation of the CRC circuit in VHDL.

Recently, parallelism in the CRC calculation becomes popular, and typically one byte or multiple bytes can be processed in parallel. A common method used to achieve parallelism is to unroll the serial implementation. Unfortunately, the algorithms used for parallelism increase the length of the worst case timing path, which falls short of ideal speedups in practice. Furthermore, the required area and power consumption increases with the higher degree of parallelism. Therefore, we seek an alternative way to implement CRC hardware to speed up the CRC calculation while maintaining the area and power consumption requirements at a reasonable level.

To remove the errors received with the data, a new approach is used called Golay encoder and decoder. The central idea of this coding technique is to retrieve or recover as much as amount of error possible to recorrect it is also correct to say is a possible ways to correct the error. To apply such coding to the system addition redundancy bits were appended with the data stream so as to facilitate, to find out or correct the errors that may have occurred. This paper present Golay codes (23) and the extended Golay code (G24) as a specific type of error-correcting codes. Three steps to transfer the information, a channel transmit, and a receiver. At the time of transmission the information is changed to noise so to avoid this condition use error correction codes.

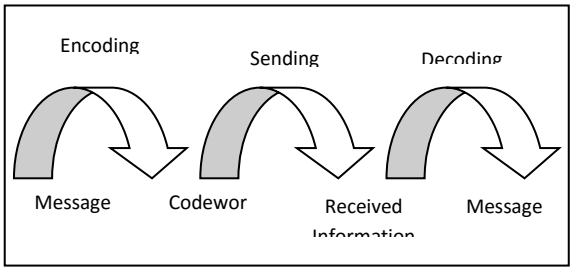

Fig. 1 message is encoded into a codeword

Fig. 1 shows the encoding procedure, in which a message is encoded into a codeword, and after encoding it is transmitted to a channel the send data may get corrupted at the time of transmission through channel because it's a wireless environment and this data is received by the receiver as corrupted data and the receiver try to recover it by using decoding process and this coding and decoding procedure is followed by the golay code in present work. The basic idea of transmitting and receiving a message is depend on which data is to be transmitted and what is received. Some golay properties is described as follow on which golay depends:

1) First property tells that out of a sequence of k symbol, message m of length k is generated so that m = (m1: mk) belongs to Fk where F is some finite field from where k symbol is selected. Then an n-code Cover a finite field F is a set of vectors in Fn, where n ≤ k. Since we will be commerce with a binary code only, we will assume codes are binary from now on.

2) Second property tells that the occurrence of error with p probability identified only when altered bit is received which means 0 is received when 1 was sent or vice versa.

3) Third property tells that a non zero function element and hamming weight of vector belongs to the function Fn.

4) Forth property tells that for achieving good response of a code calculate minimum hamming distance is one of the major concern, the humming distance of two vectors belongs to a function Fn is the number of place where they differ.

5) Fifth property tells that the minimum Hamming distance d of a code C is defined as d = min {dist(x, y) I x, y belongs to C} where c is the code.

The description of work in this paper is arranged as follows: Section-II gives an overview of the golay code. Section-III gives overview on the work performed by other scholars in Golay Code implementation and applications. Introduction on Golay code and its encoding algorithm is described in Section-IV. Section-V presents the simulation and synthesis results of the performed work. The conclusion based on the proposed work and the future work scope is presented in Section-VI. In the last the references are mentioned.

III. LITERATURE REVIEW

Reference [1, 3] is an IEEE Transaction paper which presents an efficient hardware implementation of encoder and decoder for both prototype binary Golay code (G23), extended binary Golay code (G24) based on CRC (Cyclic Redundancy Check) encoding scheme.Virtex-4 FPGA is used to design high speed with low latency architecture. This proposed method has various applications in the field of high speed communication links, photo spectroscopy, and ultrasonography. Reference [2, 8] is a paper written by Mr. Golay himself. He proposed lossless binary coding scheme to assure the reception of the correct data. To do this 23 binary symbols is used which yields the power saving one and a half db for omitting probability of errors and this code is called Golay code.

Reference [4] presents overview on Golay Complementary Sequence. These sequences are introduced by Marcel Golay in the perspective of infrared spectrometry and also give the properties and applications in different fields.

Reference [5] proposed symbol –by –symbol soft in/ soft out APP decoding algorithm for the Golay code. This decoding algorithm is suitable for convolution codes and block code with simple trellis structure. Reference [6] this paper presents the outperformance of the extended Golay code under the hard decision decoding. And compare the performance of the binary Golay code and extended binary Golay code under the ML (maximum likelihood) conditions.

Reference [7] proposed an error correction Golay code for clustering tremendous amount of Big data Streams by using error correction Golay codes and this approach is used in the field where the requirement to accumulate multidimensional data. Reference [9] proposed an efficient soft-decision decoder of the (23, 12, 7) binary Golay code up to the four errors and almost all patterns of three errors and all fewer random error can be corrected with the help of proposed algorithm.

Reference [10] presents GF (2m) Galois field encoder & decoder and its verification on FPGA using the NIST chosen irreducible polynomial. Software used to do this is Xilinx ModelSim 10.0 that simulated complete verification of multiplication& implemented on FPGA. The paper presents simple circuit and performs high speed operation by increases security during communication dialogue and decreasing the number of logic gates.

Reference [11] proposed a methodology of constructing a sequence of phase-coded waveform for which ambiguity function is free of ranges side lobes along doper shift. The problem arises with Golay code is that it has ideal ambiguity along zero Doppler-axis but is sensitive to nonzero Doppler shifts. And the application of pulse coded waveform is in the area or communication using radar. Reference [12, 14, 17, 18] proposed an algorithm for the hardware implementation of (24, 12, 8) Golay code in FPGA (Field programmable gate array) based system. To remove the complexity of arithmetic operations this arises in the existing algorithm. The proposed algorithm chooses the absolute value rather than bit error probability to obtained better results as compared to the existing algorithms.

Reference [13] proposed block product turbo code (BPTC) and simulated its efficiency. The proposed method used hamming (15, 11) and hamming (13,9) block channel code in combination to construct a BPSK modulation .This combination

gives better results and robust against BPSK Golay code and MSK Golay. Application of the proposed algorithm is in the wireless communication system Reference [15] proposes a new algorithm to fulfill the requirement of faster decoding for the Go set Lattice, Golay code and Leech Lattice. The proposed design introduced two approaches to first when charge in of length n and taking soft decoding algorithm at an arbitrary point Rn in to the nearest code word and second a decoding algorithm for a lattice A in Rn changes an arbitral point of Rn into a closest lattice point.

In Reference [16] the proposed methodology fulfil the requirement reducing the peak to average ratio (PTAR) with the help of special Fractional Fourier Transform (FRFT) followed to the low complicity Golay sequence coder in order to provide optimal de-correlation between signal and noise. To achieve the requirement of low complexity, low bit error rate and peak to average power ratio.

Reference [18] proposed a new algorithm to decode the binary systematic (23, 12, 7) and (14, 21, 9) QR codes. The proposed algorithm by using lookup table directly determines the error locations without the operation of multiplication over a finite field. The reason of using the FLTD is the CPU time is half of the LTD algorithm.

IV. PROPOSED METHOD

A. Golay code Encoder Algorithm

(23, 12, 7) represents a binary Golay code here all the three values have different meaning like 23 means there is a codeword having length of 23 bits. 12 represents length of the message is of 12 bits and 7 represents minimum distance between two binary Golay codes. Now it is interesting to know that the construction of binary code done in Galois Field which is denoted by GF (2), which supports different binary arithmetic operations. The generation of the code sequence is achieved by Generator polynomial. The possible generator polynomials over GF (2) for Golay (23, 12, 7) code are :x11 + x10 + x6 + x5 + x4 + x2 + x1 And x11+ x9+x7+x6+x5+x1+1

This Generator polynomial is used to encode a 12-bit binary number into a 23-bit Golay code. And to achieve this long division is performed and the results of the long division generate check bits (11-bit). Therefore the 12-bit information data is converted to 23 bit golay code by appending 11 bit to the 12 original data. And the extended Golay code (24, 12, 8) can be generated by appending a parity bit with the binary Golay code or using a generator matrix G, which is defined as [I, B] or [B, I], where I denotes an identity matrix of order 12. The matrix B is shown in fig. 2. Bi represents ith row of the matrix B.

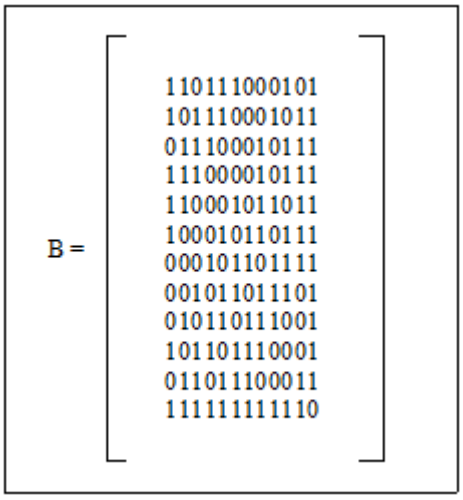

Fig. 2 Matrix-B

The algorithmic steps followed to accomplish the encoding process are enlisted below:

1) Characteristic polynomial is selected for check bits generation
2) The data of length 'M' participate in long division method with the characteristic polynomial. So, 11 zeros are appended to the right of data message M.
3) The check bits for G23 are the most significant bit (MSB) resulted at the end of the division operation.
4) The encoded Golay (23, 12, 7) codeword are received by appending check bits with the message.
5) A parity bit is appended to convert the binary Golay code into extended binary Golay code (24, 12, 8). If the weight of binary Golay code is odd, then parity bit 1 is appended, otherwise 0 is appended.

Figure3 presents an example of the function performed to generate redundant bits. The function performed in this example to generate

redundant bits of 11-bits is long division method by taking 12-bit data 111001100111 and the characteristic polynomial is 101011100011. The golay encoder is of 23-bit (G23) is 111001100111-00011001010. And to convert the golay code to extended golay appending parity bit in it. In the G (23) word the weight is 11, i.e., the encoded word has 12 1's, so a 0 will be appended in it. This will generate extended codeword G (24) as (111001100111-00011001010-0).

Data (12-bit)	Appended zeros	Encoder Operation
111001100111	00000000000	
101011100011		... xor
0100100001000		... 1-time shift
101011100011		... xor
001111010 1100		... 2-time shift
101011100 011		... xor
010101001 1110		... 1-time shift
10101110 0011		... xor
00000111 110100000		... 5-time shift
101011100011		... xor
0101010000110		... 1-time shift
101011100011		... xor
000011001010		... 1-time shift
<Check-bits>		

Fig.3 Long Division of Data for Check bits generation

The parity bit generation is implemented by XOR-ing the bits of G (23) codeword. This is depicted in fig. 4.

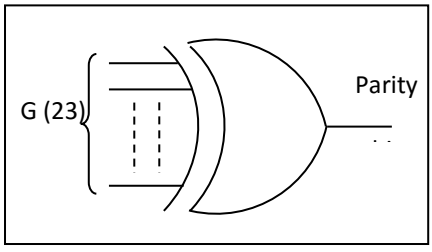

Fig.4 Parity Bit Generation using XOR-ing operation

The weight of the G(24) code work is 12 by appending a parity bit in to it which is the basic difference between golay and extended golay code and this 12 bit weight validate the extended golay code. In extended golay code the validity of code is check by a condition and the condition is the weight is multiple of 4 and greater than or equal to 8.In the given example, the weight of the G (24) codeword is 12, so it is a valid codeword.

B. Golay code Decoder Algorithm

Imperfect Maximum Likelihood Decoder (IMLD) based decoder implementation and simulation is performed. The algorithm that is used to implement the design is defined below:

1) Calculation is performed to calculate syndrome 'S' from the received code word 'W' and matrix 'H',where H = [I / B]
2) Check condition performed to give the error free data. And the condition is express as wt(S) ≤ 3where wt is weight of 'S'., E = [S, 0]is error vector.
3) If wt(S+Bi) ≤ 2, then E = [S+Bi, Ii]. Where Ii represents ith row of the identity matrix I.
4) Calculate SB, SB is the second syndrome.
5) If wt(SB) ≤ 3, then E = [0, SB]
6) If wt(SB+Bi) ≤ 2, then E = [Ii, S+Bi]
7) The retransmission condition occurs only when E is not determined.

The algorithm assumes that 'E' be the error pattern of the received codeword 'W'. S and SB were the two syndromes that are calculated using the received codeword. Syndrome S is calculated by applying multiplication of received codeword W with parity check Matrix 'H' which is given by as [I, B] or [B, I]. Therefore, the12- bits syndrome 'S' of a word 'W' evaluated by syndrome measurement equations as shown in fig. 5. And in decoding process the error pattern identified by the weight of (S + Bi) and (SB + Bi). Simplified adder based architecture is implemented in this work to calculate the weight of a 12-bit (S + Bi) and (SB + Bi), for 1≤i≤12. The architecture of adder based weight calculation unit is shown in fig. 5.

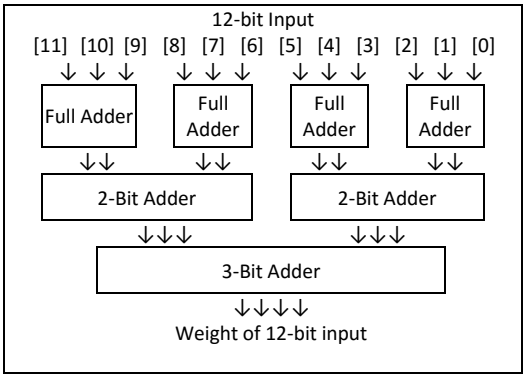

Fig. 5 Architecture of Weight Calculation Unit

Simulation and Synthesis Results

The present work is simulated using Xilinx. The RTL Schematic diagrams of Encoder and Decoder designs are shown in Fig-6 and Fig-7 respectively.

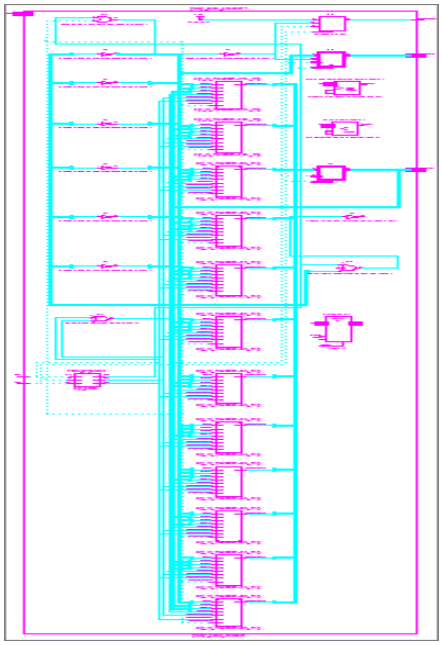

Fig. 6 RTL Schematic Diagram of Proposed Golay Code (24, 12, 8) Encoder

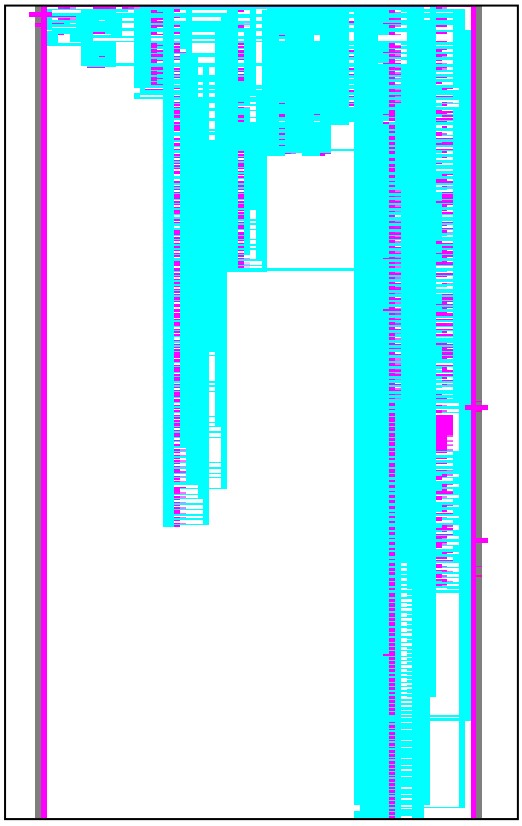

Fig.7 RTL Schematic of Proposed Golay Code (24, 12, 8) Decoder

The Encoder and Decoder simulation waveforms are shown in Fig-8 and Fig-9 respectively. A 12-bit data is used to encode using the proposed encoder. The input data bits are followed by logic-'0' inputs.

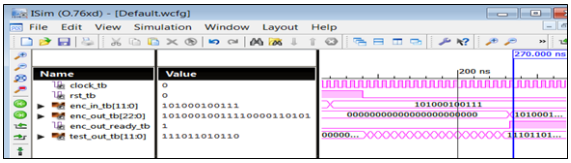

Fig. 8 Encoder Simulation Waveform for Proposed Golay Code (24, 12, 8) Encoder

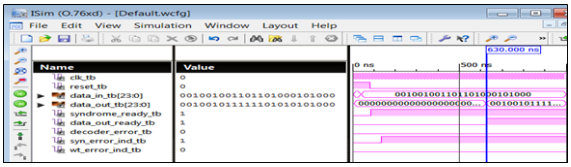

Fig. 9 Encoder Simulation Waveform for Proposed Golay Code (24, 12, 8) Decoder

The FPGA based hardware utilization summary of the proposed Encoder and Decoder designs is presented in Table-I and Table-II respectively. Table-III represents a comparative analysis of the delay based results of the proposed work with some existing works.

TABLE I: Hardware Utilization Summary of Encoder

Vertex-IV XC4VLX160 -12FF1148	**Total**	**12-bit Golay Encoder**	
		Used	**%**
Slices	67584	47	0
Flipflops	135168	44	0
LUTs 4-Inputs	135168	89	0
Bonded IOBs	768	50	6

TABLE II: Hardware Utilization Summary of Decoder

Vertex-IV XC4VLX160-12FF1148	**Total**	**12-bit Golay Decoder**	
		Used	**%**
Slices	67584	360	0
Flipflops	135168	305	0
LUTs 4-Inputs	135168	695	0
Bonded IOBs	768	55	6

TABLE III: Frequency comparison of Proposed Design

Work	Operational Frequency (MHz)	
	Encoder	Decoder
Proposed	383.245	311.491
[1]	238.575	195.082
[5]	-	100

Conclusion

Delay optimized hardware architecture for extended binary Golay encoder and decoder are designed and simulated in the proposed work. The results obtained from the design synthesis for encoder and decoder supersedes the reference schemes in term of the operational frequency. This makes the proposed design a good option to be used in the high speed application based configurable circuits. In future there is a great scope to further optimize the performance of the proposed algorithm. In future the scholars may undertake the challenge to reduce the ratio of overhead bits versus data bits in the encoded codeword. Or the researchers might increase the length of the data word that can be encoded using the same algorithm with the same or better error detection and correction ability.

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