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REVIEW ARTICLE

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A REVIEW ON SIMULATION OF 'QPSK' USING 'VHDL'

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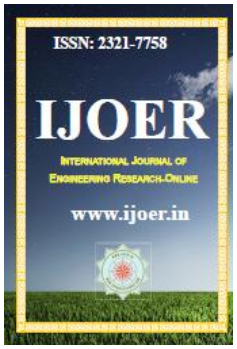

ABSTRACT

QPSK (Quadrature Phase Shift Keying) is one type of digital modulation technique used to transfer the baseband data wirelessly in much efficient way compare to other modulation techniques. Conventional VHDL implementation of QPSK modulator has some limitation with respect to size, speed and power consumption, the main purpose of this work is to design the QPSK system in VHDL with the help of VHDL simulators such as Xilinx ISE etc. Two new types of QPSK modulator have proposed to design. The developed method considered eliminate the generation of 2 phases and produced the QPSK output based on stored data in RAM. The conventional method used to generate the QPSK signal consumes high power and area efficient. The developed QPSK modulators are fully digital domain and produced QPSK output same as standard QPSK. The modulated signal obtained from simulations was compared with the signal obtained after implementation.

Keywords: Very high speed hardware description language (VHDL), quardrature phase shift keying (QPSK), Random access memory (RAM), Read only memory (ROM).

I .INTRODUCTION

There is an increasing need to process, interpret and understand information due to the increasing use of computers. And because of these, the usage of and need of digital signal processing has increased. DSP functions are commonly implemented on two types of programmable platforms. Digital signal processors are a specialized form of microprocessor, while FPGAs (Field

Programmable Gate Array) are a form of highly configurable computing. Although digital signal processors are programmable through software, their hardware architecture is not flexible, while FPGAs provide a reconfigurable solution for implementing DSP applications so in recent years, FPGAs became an essential part in implementing DSP (Digital Signal Processing) systems, especially in areas such as digital communications. Among available tools for FPGA design, System Generator is a system-level modelling tool that facilitates Xilinx FPGA hardware design in Simulink and Matlab. The aim of this paper is to test the functionality of two digital designs, the QPSK systems, using simulation provided by System Generator.

QPSK modulation ordinarily use modem chips, or ASIC to implement, but those chips usually don't have sufficient Programming skills and its functionality cannot easily be changed or improved in the product development process. Therefore, those chips are not suitable the situation where the parameters changed frequently. The communication system based on FPGA is easy to implement the pipeline architecture and simple to upgrade. This is a

very practical approach to implement the QPSK modulator.

The conventional method used to generate the QPSK signal consumes high power and area efficient. The developed QPSK modulators are fully digital domain and produced QPSK output same as standard QPSK. The two new developed QPSK modulators used RAM as main data storage to produce same QPSK signal as conventional modulator

II . RELATED WORK

1] Silvana Popescu, Aurel Gontean, Georgeta Budura Applied Electronics Department, Faculty of Electronics and Telecommunications, Politehnica University of Timisoara, Timisoara, Romania had implemented digital signal processing solutions using FPGAs. The hardware designs of the QPSK systems, using Matlab/Simulink environment, System Generator and Xilinx ISE, in order to verify the functionality of the systems in hardware which speeds up the simulations. The capabilities of the Spartan and conclude that the time taken to simulate is less.

2] Wenmiao Song and Qiongqiong Yao Dept. of Electronic & Communication Engineering North China Electric Power University China proposed a method to designs QPSK modulator and demodulator of a spread spectrum system which use field programmable device. The method uses the tool of Quartus of American Altera Co. The whole system is divided into several small models based on top-down design method, and using VHDL hardware description language to design each model and conclude that the method can greatly improve the developing efficiency, shorten developing period and reduce costs.

3] Gihad Elamary, Graeme Chester, Jeffrey Neasham Proceedings of the World Congress on Engineering London, U.K. proposed a new simple design for a Quadrature Phase shift Keying (QPSK) modulator applied for implantable telemetry applications as demonstrated. VHDL programming code is used to generate QPSK digital signal. The input test signals data and carrier are interfaced to the CPLD and FPGAs board from Agilent function generator (E8408A) and used the local clock oscillator for test, which is operating at 25.175 MHz and used 12.5MHz for the carrier and 2Mbps reduced for data source. And concluded that The output producing modulated digital signal, filtered to transmit through designed filters (LPF/BPF) at carrier frequency 12.50 MHz and data rate 2Mbps. Which presents better performance with high data rate and carrier suppression about 40dB.

4] Miichal Kovac and Jaromir Kolouch proposed the modulator in the FPGA using VHDL language and DDS component in the Xilinx ISE The reason why an FPGA was used is that the FPGA is highly configurable silicon engine, with high MIPS (Mega Instruction Per Second) real-time signal processing functions. Compared to the digital signal processors (DSP), FPGA are characterized by a high flexibility. Conclude that revolutionary evolution in FPGA technologies allowed increasing gate count, clock speed and integration of many functions like dedicated high-speed hardware multipliers and embedded processors.

5] Kavita A. Monpara, Shailendrasinh B. Parmar Electronics and Communication Department, Shantilal Shah Engg. College, Bhavnagar, Gujarat Technological University Gujarat, implemented QPSK modulator is developed for satellite communication for future satellite missions. As knowing that for space application power and bandwidth are most important parameters. The size of PCB and component count are also important parameters. To reduce these all parameters we design new approach. The new approach also minimizes the component count and hence reduces the PCB size. In this modulator summation, orthogonal sub-carrier generation and mixing of subcarrier with data are all digitally implemented inside the FPGA. This modulator, analog components like local oscillator and mixer are completely eliminated which are frequency and temperature sensitive. Here all the functions are performed by single FPGA. So the limitations of modulator are completely removed for satellite communication. For the satellite communication PCB size is also important parameter and using this new approach number of component count is less and ultimately size of PCB is become small.

6] Tushar V. Kapare Electronics and Communication Department, GHRCEM Pune implemented a simulation low power of QPSK on FPGA and developed a system to modulate the data for communication so that to provide security for data as well as to enhance the communication data rate and the system is implemented on Spartan3 provided by Xilinx so that to minimize the power required and the speed of communication is increase.

7] Asharad Mohammad Moubarak, Mohd Allaudin Mohd Ali, Hilmi Saunsi and saval Mohd Ali faculty of Electrical and Electronics Department, University of Kebansang Malaysia implemented a system on low power digital QPSK modulator using a VHDL and concluded that the propose system consume the less power as compared to conventional system and the less power consumption is achieved due to the less usage of input and output block .

8] Wen Wu department of signals and systems division of communications systems Chalmers university of technology implemented a FPGA-based 5 Gbit/s D-QPSK Modem and developed a Differential Quadrature Phase Shift Keying (D-QPSK) modem supporting 5 Gbps (Gigabits per second) data rate transmission. A 2.5 Gbps field programmable gate array (FPGA)-based modem had been designed and verified previously. This modem was built using FPGA and microwave components, in which the FPGA is programmed to generate a D-QPSK signal and the microwave components perform the up-and down-conversion between baseband and intermediate frequency (IF) signal and concluded that no need for carrier recovery in non-coherent detection however, data clock recovery (DCR) is needed for clock alignment with the output 5 Gbps serial data.

9] Teena Sakla, Kumhar Mohalla Bairagarh, Divya Jain, Sandhya Gautam Technocrats Institute of Technology Bhopal implemented Digital QPSK Modulator by using VHDL to reduce the channel distortion and to use in RF communication and in communication system to transmit the data through channel without loss of data and to reduce size of antenna incase of wireless communication. The model involves a FPGA based 4X1 multiplexer, one clock & four delay blocks to produce four phases then the output is filtered by the analog filter to produce smooth sinusoidal wave at the output and the system is cheap in cost, better stability and less complexity.

III. PROBLEM FORMULATION

After studying the various work QPSK Modulator there is Continuous growing demands from end user for more data have encouraged the engineers to develop many new types of modulation scheme in communication system. New types of modulation technique introduced to increase the efficiency in data transmitting and receiving rate within the same bandwidth. One of the common modulation method used in communication system is QPSK which is one form of PSK (Phase Shift Keying) modulation scheme but the conventional QPSK modulator operates by dividing the baseband data into 2 main streams, even and odd data. The divided unipolar data then changed into bipolar by using NRZ encoding technique. For this there required a more logical element so it has a more power consumption.

IV. CONCLUSION

As per the review of Simulation of QPSK in VHDL it is concluded that QPSK is efficiently used in communication with the low power consumption with using the less number of logical element.

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