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RESEARCH ARTICLE

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SIMULATION OF QPSK USING VHDL

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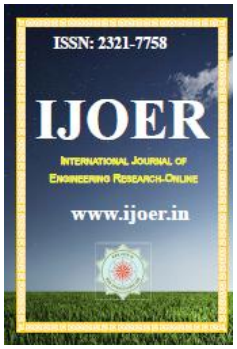

ABSTRACT
In many applications such as TDMA cellular telephone, OFDM, Bluetooth, Satellite communication etc. QPSK digital modulation technique is used due to its higher bandwidth efficiency, higher noise immunity and simpler circuit. Simpler circuit is having lower cost, smaller size and lower power dissipation. In this paper a new circuit for QPSK modulator is designed which improves the area of the circuit. It is having lower logic elements than conventional design which provide same output. The circuit designing is performed on Active-HDL9.2 and implemented on Spartan II (XC2S30-5PQ208) FPGA board using Xilinx ISE9.1i and results are observed on laptop using Xilinx 9.1i VHDL simulator. The area of the design is found to be lower in total logic elements than the conventional design.
Keywords- QPSK, FPGA, ROM, Flip-Flops, Modulation etc.

1. INTRODUCTION

In satellite communication, modulation is necessary to transfer the information between satellite and the earth. There are basically two types of modulation technique analog modulation and digital modulation. From these two modulation technique digital modulation technique have several advantages over analog modulation technique like less interference, greater fidelity, robust, high S/N ratio etc. So in satellite communication generally digital modulation is used. In digital modulation technique, there are several types of modulation techniques are present like ASK (Analog shift Keying), FSK (Frequency Shift Keying),PSK (Phase Shift Keying) etc. All these have own advantages and disadvantages. In satellite communication power, bandwidth and size of circuit are very important parameter. This parameter must be maintained for on board processing system in satellite communication. Now in satellite communication power is severally limited. For the satellite communication FSK is not generally used as it would require very high bandwidth to modulate our data resulting in very low bandwidth efficiency. Higher constellation QAM also can't be used in satellite communication as that would require very high C/N ratio. The choice is between QPSK and BPSK. The advantage of BPSK is that it requires the lowest C/N ratio. The drawback is that the data rate achieved using BPSK is very low. QPSK is basically two BPSK links operating on the same radio channel with their carriers in phase quadrature. Therefore the BER of a QPSK remains the same as BPSK. At the same time the data rate is doubled. MSK is also one type of PSK technique, but for this we require complex circuit and higher bandwidth than QPSK. Our project demands high data rate without losing much on bandwidth and power. Because of these tradeoffs we decided on using QPSK modulation scheme for application of satellite communication. Now today in satellite communication for on board processing system QPSK modulator is used but in this

modulator analog components are used like local oscillator, mixer, 90° phase shifter. All these components are frequency and temperature sensitive. Also the no. of components are higher so size of PCB require for this modulator is comparatively high. So after few years the performances of these components are degrading. And ultimately this effect on the performance of QPSK modulator and this degrades the performance of satellite communication. So our aim to design such a modulator circuit which eliminates all these limitations of today's modulator circuit used in satellite communication. Here we design completely digital QPSK modulator. In our circuit we eliminate the use of local oscillator, mixer, 90° phase shifter. The functions of all these components are performed by FPGA. Here carrier is digitally generated using LUT (Look Up Table). Now FPGA is digital component which is frequency and temperature insensitive. So the performance of this modulator cannot degrade as time passes. And also the number of component is reduced and ultimately size of PCB is reduced. Limitations of today's modulator which are used in satellite communication are eliminated.

2. CONVENTIONAL MODULATOR

A. The model-The QPSK modulator can modulate two signals in same frequency band. Each signal is to be converted from analog to digital, this digital signal is encoded by encoder then modulation is takes place. One signal is modulated with sine and another with cosine which gives four (two of each) different phases, by adding these two phase shifted signals we get QPSK output signal [1].The above figure shows the block diag. of conventional QPSK modulator in which spconv2 (serial to parallel converter) block takes data (d) as input and separate it into two signals Q and I. There are two BPSK blocks, sin_inv11 and cos_inv11. Each block is consisting of a ROM, Subtracted and MUX which generate BPSK output waveform. ROM block give sine wave, subtracted give inverse sine wave and MUX block select each one according to sel input i.e. for sel as '0', sin block produce sine waves and for '1' it gives invert sine wave similarly for cos block. These four combinations of two inputs are added into adder block to produce QPSK as output waveform. It consists of total 9 bits (8 bits data and 1 bit carry). Carry bit is generated due to addition of two 8 bits data signal.

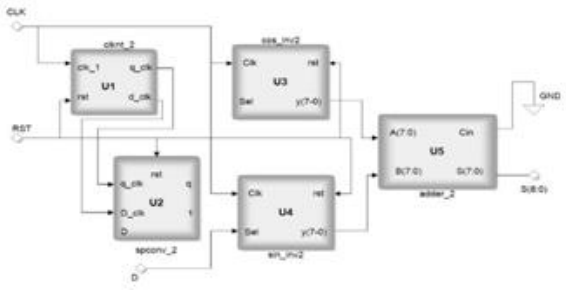

Fig. 1 Conventional QPSK Modulator with two ROMs

B. Mathematical equation of QPSK Modulator

The QPSK signal can be given as

$S_{QPSK} = \sqrt{2E_s/T_s}\, COS(2\pi f_c t + (2i-1)\,\pi/4)$For i = 1, 2, 3, 4..., Where, $\sqrt{2E_s/T_s}$ Constant amplitude with *Es* energy and *Ts* time period of the signal, f_c= Frequency of carrier signal, *i*= phase no. of signal as per the symbols of the data signal from the trigonometric equation given below,

cos(*A*+*B*) = cos(*A*)cos(*B*) - sin(*A*)sin(*B*) ……(2) from eq. (2) we can write,

$S_{QPSK} = \sqrt{2E_s/T_s}\, cos(2\pi f_c t)\cos[(2i-1)\,\pi/4)]$- $sin(2\pi f_c t)\sin[(2i-1)\,\pi/4)]$ ……(3)

Fig.1. Shows that separate sine and cosine waves are generated which require two ROM's to store these signals [2]. They are then modulated by the input binary data signal. These two signals are then added to generate the QPSK signal. All these process is discuss in [5] with design flow diagram. There are two signals in QPSK signal i.e. in-phase I(t) and Quadrature Phase Q(t). Which is given in eq. (3) can be written as

$S_{QPSK} = \sqrt{2/T_s}\, cos(2\pi f_c t)\mathrm{I}(t))$- $\sqrt{2/T_s}\, sin(2\pi f_c t)\mathrm{Q}(t))$, where, I(t) = $E_s \cos(2i-1)\,\pi/4$ and ,

Q(t) = $E_s \sin(2i-1)\,\pi/4$Output QPSK waveform with four different phase shifts isas shown in figure 2. In this, we can see that for eachsymbol phase

angle of original signal is different.Fig. 2 Output waveform of QPSK modulator in time domain.

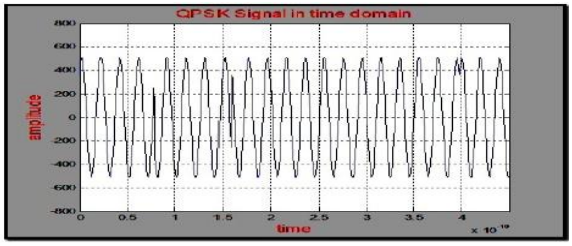

Fig. 2 Output waveform of QPSK modulator in time domain

3. PROPOSED WORK

We know that, day by day electronic devices are getting smaller in size also reduction in its cost. It means the area is one of the main factors while designing digital circuit. The required amount of components for any circuit should be as less as possible which produce same output. While designing any circuit all the other factors such as power dissipation, capacitance, clock timing etc. needs to consider and assure that all these factors are in certain limit. In this paper main focus is given on reducing the actual size of conventional QPSK Modulator by reducing the no. of logic elements in the design. From eq. (1) we can say that SQPSK is having only costerm, it means output waveform is consist of only cosine wave with different phase shifts according to variable 'i. Considering this factor, a ROM is developed which will generate only cosine wave with different values of 'i' taken as symbol or combination of Q and I i.e. 4 values. As shown in fig above the sin_inv11, cos_inv11 and adder are replaced by single block i.e. rom8. It takes Q and I as two input signals. According to change in input there will be change in phase of signal. As shown in fig above the sin_inv11, cos_inv11 and adder are replaced by single block i.e. rom8.

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Rom8block is having 64different values of a sin wave. The particular symbol(combination of Q and I) starts the waveform from particular value for that phase. After that, sine wave continues until there is change in symbol. In this case thereis no addition of two waves hence the output is of 8 bits and there is no carry.

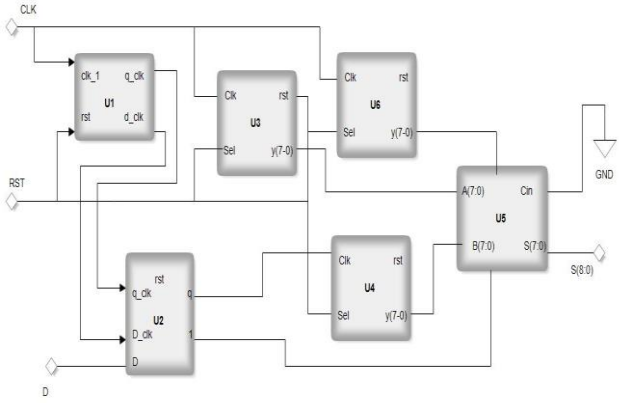

Fig. 3 Proposed QPSK Modulator with diff data ROM

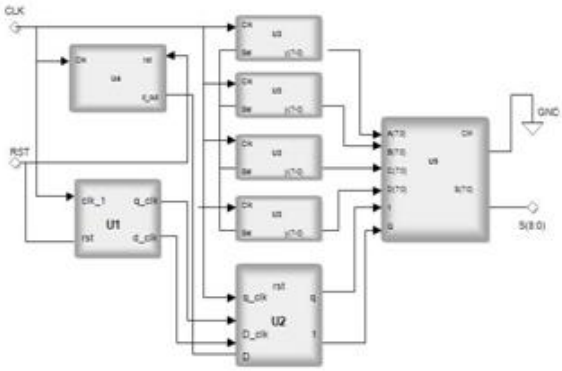

Fig. 4Proposed QPSK Modulator with 4:1 MUX.

Below table shows that, the phase change of the signal is depend on the change in symbols, each symbol is having particular phase angle or signal pattern. In ROM these phases are achieved by selecting different symbols and starting the wave from particular value. The output waveform of proposed blocks, which is as shown below which is similar to the conventional modulator waveform. It shows same phases for each symbol.

Table1 shows that, the phase change of the signal is depend on the change in symbols, each symbol is having particular phase angle or signal pattern. In ROM these phases are achieved by selecting different symbols and starting the wave from particular value.

Table I: Phase shifted signal for different input symbols

Symbol	Bits	S(t)	Phase (Deg.)	Mod. Signal
S1	00	$\sqrt{2E_s/T_s}\,COS\,(2\pi f_c t) + 5\pi/4)$	225^0	
S2	01	$\sqrt{2E_s/T_s}\,COS\,(2\pi f_c t) + 3\pi/4)$	135^0	
S3	10	$\sqrt{2E_s/T_s}\,COS\,(2\pi f_c t) + 7\pi/4)$	315^0	
S4	11	$\sqrt{2E_s/T_s}\,COS\,(2\pi f_c t) + \pi/4)$	45^0	

4. RESULTS AND DISCUSSION

There are total two different designs, one for 16 values ROM of conv. and proposed architecture are discussed in this paper and their device utilization are as shown below. From results, we can see that design 2 is having lowest logic elements as compared to others. Design 1 shows large difference between all the parameters than design 1 and also design 2. From this we can say that design 2 is better in area utilization than design 1, while the design 2 is best among all. In this way the smaller size of QPSK modulator has achieved in proposed architectures. Design 1 is having total 64 values in their ROMs which take 64 clock pulses to read the one waveform data(data to produce one wave) whereas design 1 and 2 is having 16 ROM values and require 16 clock pulses. The speed of the design is depends on clock timing and the clock timing is depend on physical parameters in the circuit such as capacitance, inductance, loading resistance etc. All these parameters are affected by the area of the design. From this we can say that the speed of operation is depends on the size or area of the design. The comparison of clock timing (ns) of all the designs is as shown below Design 1 takes 3.433ns less time than design 2, since it is having larger size than design 2.Conventional designs are taking somewhat lesser time than proposed one but it is having larger size. The comparison of power dissipation of all the designs is as shown below, in above figure, design 1 and 2 is having lowest power dissipation while it is having highest clock timing, as power dissipation depends on it, higher the clock timing lower is the speed of operation and lower the power dissipation.

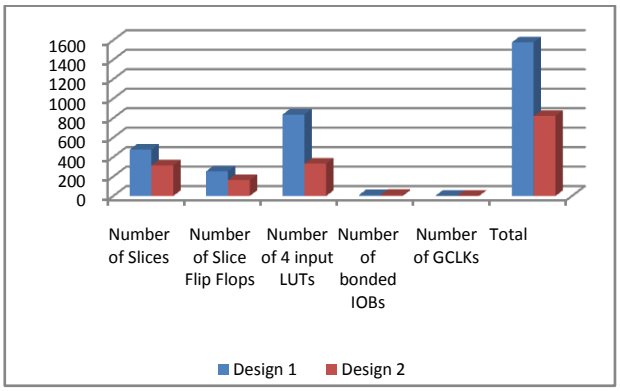

Fig. 5: Device utilization summery

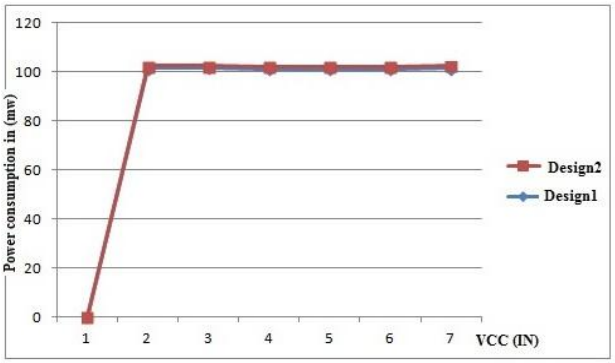

Fig. 6: Power dissipation of different designs

5. CONCLUSION

Here, we design digitally QPSK modulator. In this modulator, analog components like local oscillator and mixer are completely eliminated which are frequency and temperature sensitive. Here all the functions are performed by single FPGA. So the limitations of modulator are completely removed for satellite communication. For the satellite communication PCB size is also important parameter and using this new approach number of

component count is less and ultimately size of PCB is become small.

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