International Journal of Engineering Research-Online
A Peer Reviewed International Journal
Email:editorijoer@gmail.com http://www.ijoer.in

Vol.4., Issue.3., 2016
(May-June)

RESEARCH ARTICLE

ISSN: 2321-7758

DESIGN AND DEVELOPMENT OF A NEW SINGLE-PHASE SOFT SWITCHING POWER FACTOR CORRECTION CONVERTER

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ABSTRACT

Losses occur, when converters are operated at high frequency. This paper presents, single-phase soft-switching power factor correction (PFC) converter with a new active snubber circuit. The main switch is turned on and off with zero voltage transition (ZVT) and zero current transition (ZCT) respectively without any additional stresses of voltage and current on the main switch. Auxiliary switch is turned ON and OFF with zero-current switching (ZCS) without additional voltage stress. Although, there is a current stress on the auxiliary switch, it is decreased by diverting a part of the current to the output side with coupling inductance. The output current and voltage are controlled by the proposed PFC converter with different load ranges. The simulation part is done with Matlab Simulink.

Keywords- Power factor correction (PFC), soft-switching (SS), zero-current switching (ZCS), zero-current transition (ZCT), zero-voltage switching (ZVS) and zero-voltage transition (ZVT).

I. INTRODUCTION

The electricity networks have various drawbacks - i) Very poor power quality in terms of injected current harmonics which results in voltage distortion ii) At input AC side a poor power factor iii) Slow varying ripples at dc output load, low efficiency and iv) Large size of AC and DC filters which is due to the AC-DC converters used in the power electronic systems which introduces harmonic currents from the ac mains. The power electronic systems and devices, which are used more frequently, create harmonics current and pollute the electricity network. Harmonics have a negative effect on the operation of the receiver, which is fed from the same network. Nowadays, engineers design all the electronic devices to meet the harmonic standards. When these AC-DC converters are operated at high-switching frequency it results in higher switching losses, increased electromagnetic interference (EMI), and reduced converter efficiency. To overcome these drawbacks, low harmonic and high-power factor converters are used with soft-switching (SS) techniques. High-switching frequency with SS provides high power density, less volumes and lowered ratings for the components, high reliability, and efficiency.

The switching power losses consist of the current and voltage overlap loss during the switching period, power diode's reverse recovery loss and discharge energy loss of the main switch parasitic capacitance. SS with pulse width modulation (PWM) control has four main groups as zero-voltage switching (ZVS), zero-current switching (ZCS), zero-voltage transition (ZVT), and zero-current transition (ZCT). ZVS and ZCS provides a SS, but ZVT and ZCT techniques are advanced, so switching power loss can be completely destroyed or is diverted to entry or exit. In the converter, ZVT turn ON and ZCT turn OFF together for the main switch and ZCS turn ON and turn OFF for the auxiliary switch without an important increase in the cost and complexity of the converter. There are no additional current or voltage stresses on the main switch. A part of the current of the auxiliary switch is diverted to the output with the coupling inductance, so better SS condition is provided for the auxiliary switch. In this analysis the aim of proposed circuit is to achieve high efficiency and high-switching frequency PFC converter through Matlab.

II. OPERATION MODES AND ANALYSIS

A. *Definitions and Assumptions*

The proposed new single phase soft switched PFC converter circuit is given in Fig: 1.In this circuit V_i is input dc voltage, V_o is output voltage, L_F is main inductance, C_o is output capacitor. PMDC motor is output load, S_1 is the main switch, S_2 is the auxiliary switch, and D_F is the main diode. The main switch consists of a main switch S_1 and its internal body diode D_{S_1}. C_S is the sum of the parasitic capacitors of the main switch and the main diode, so it is not an additional component to the proposed converter. L_{R1} is upper snubber inductance and L_{R2} and L_{R3} are lower primary and secondary snubber inductances, C_R is snubber capacitor, and D_1, D_2, D_3, and D_4 are the auxiliary diodes. In Fig.1, i_s is input current, I_i is main inductance current, i_{S_1} is main switch current, $i_{L_{R1}}$ is L_{R1} inductance current, $i_{L_{R2}}$ is L_{R2} inductance current, i_{S_2} is auxiliary switch current, i_{D_F} is main diode current, and I_o is output current. V_{C_S} and V_{C_R} are C_S and C_R voltages, respectively.

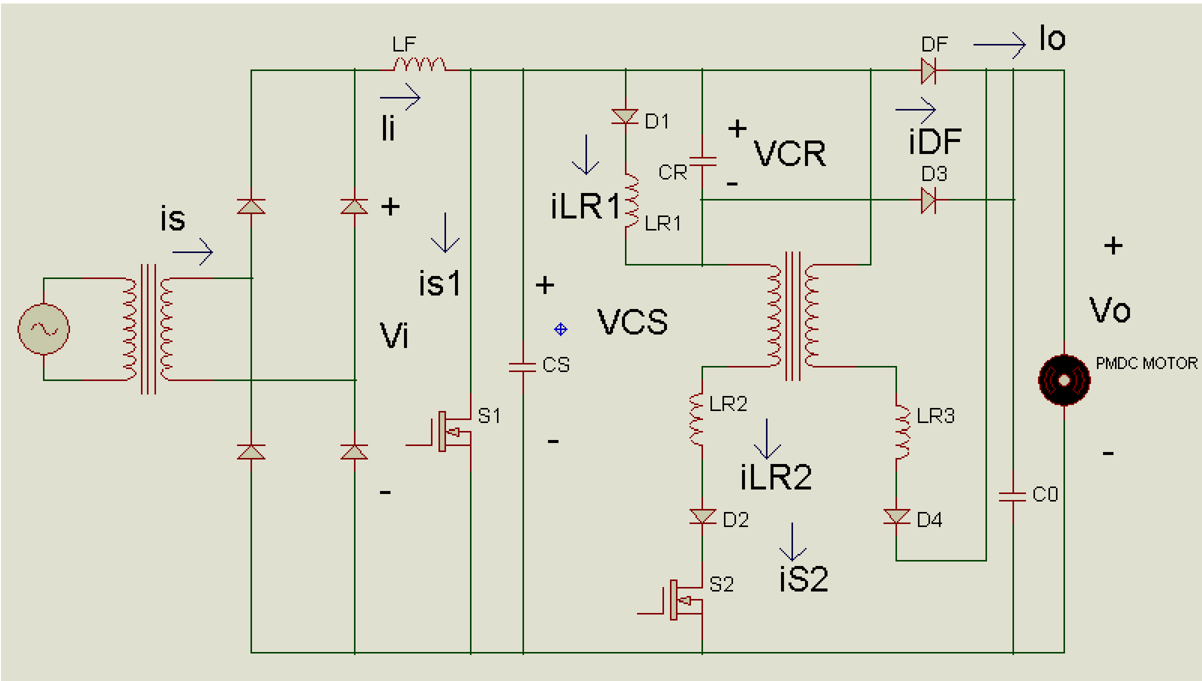

Fig: 1 Circuit scheme of the proposed new PFC converter.

B. *Proposed Circuit Analysis*

Twelve stages occur over one switching cycle. For one switching cycle, following assumptions are made:

Output voltage V_o and I_i are constant for one switching cycle. All semiconductor devices and resonant circuits are ideal. The reverse recovery times of all diodes are not taken into account.

Stage1: First switches S_1 and S_2 are in the OFF state. During this time input current passes through the D_F main diode. When the gate signal is applied to the switch S_2, a resonance starts between

L_{R1},L_{R2},L_{R3} and C_R. Then, S_2 current rises and D_F current falls.

L_{R2} and L_{R3} snubber inductances provides turn ON switching with ZCS of S_2, D_1 and D_2. When the sum of the input and output currents of transformer reaches input current I_i, the D_F current falls to zero and turns OFF with ZCS.

Stage2: The switch S_1 and the diode D_F are in OFF state, S_2 in ON state. Resonance starts between C_S, L_{R1}, L_{R2},L_{R3} and C_R. The capacitor C_S discharges, at the same time stored energy in L_{R2} and L_{R3} are transferred to the output side by coupling inductance. V_{C_S} becomes zero, D_{S_1} turns on and meanwhile D_4 turns OFF.

Stage3: D_{S_1} is turned on. The resonant between L_{R1}, L_{R2},L_{R3} and C_R continues. In this stage, D_{S_1} diode conducts the excess of L_{R2} and L_{R3} currents from the input current. The interval of this stage is time for the main switch S_1 to turn on with ZVT. During this ZVT time, gate signal must be applied to the main switch S_1. So S_1 can be turned on with both ZVS and ZCS by ZVT.

L_{R2} current drops to the input current, so D_{S_1} turns off with ZCS and S_1 turns on with ZVT. The main switch current starts to rise. S_1 current reaches to the input current level and L_{R2} current becomes zero. When the auxiliary switch current becomes zero, it is time to cut off the gate signal of S_2. So, the auxiliary switch S_2 perfectly turns off with ZCS

Stage4: S_2 switch is turned off. While S_1 conducts input current Ii, a resonance occurs through L_{R1}, C_R and D_1. The energy in L_{R1} is transferred to the CR with this resonant. This stage ends when L_{R1} current is equal to zero and C_R voltage reaches its maximum level.

Stage5: The main switch S_1 conducts input current Ii and the snubber circuit is not active. The duration of this interval is a large part of the on state duration of the boost converter and is determined by the PWM control to provide PFC.

Stage6: When the control signal of the auxiliary switch S_2 is applied, a new resonance starts between C_R,L_{R2},L_{R3},S_2 and S_1. The auxiliary switch S_2 turned on with ZCS through L_{R2} and L_{R3} . The auxiliary switch current rises and the main switch current falls due to the resonance.

When the S_2 current reaches input current level, the main switch current becomes zero. After S_1 current falls to zero D_{S_1} is turned on with ZCS. There is zero current and zero voltage on the main switch S_1. So it is time to cut off the gate signal of S_1 to provide ZCT.

A new resonance occurs through the way of C_R,L_{R2},L_{R3},S_2 and D_{S_1}. D_{S_1}conducts the excess of $i_{L_{R2}}$ and L_{R3} from the input current. V_{C_R} falls to zero and $i_{L_{R2}}$ current reaches its maximum levels.

Stage7: While V_{C_R} voltage starts to be positive, D_1 diode is turned on. A resonance starts between L_{R2}, L_{R3},L_{R1} and C_R. L_{R2} current falls again to I_i and D_{S_1} current becomes zero. The diode D_{S_1} turns off with ZCS. The duration of the on time of the $D_{S_1}$is equal to the ZCT time.

Stage8: Because $i_{L_{R2}}$ current falls to I_i, a resonance occurs between C_S, L_{R1}, L_{R2}, L_{R3} and C_R with this current. The $i_{L_{R2}}$ current falls, and when $i_{L_{R2}}$ current is equal to zero, S_2 can be turned off. So the auxiliary switch S_2 is turned off perfectly under ZCS.

Stage9: There are two different closed circuits for this stage. For the first closed circuit, C_S capacitor is charged linearly with I_i and for the second closed circuit, a resonance occurs through L_{R1}, C_R and D_1. The sum of V_{C_S} and V_{C_R} voltages is equal to V_o, so D_3 diode can be turned on.

Stage10: A new resonance occurs through L_{R1},C_S and C_R with I_i input current. The $i_{L_{R1}}$ current falls to zero, so this interval ends. The energy stored in L_{R1} inductance is transferred to the capacitors and load completely.

Stage11: C_S is charged linearly with constant I_i current and C_R is discharged. When C_S capacitor voltage reaches to V_o, C_R capacitor voltage falls to zero and D_F diode is turned on with ZVS.

Stage12: The main diode D_F conducts input current Ii and the snubber circuit is not active. This time period is determined by the PWM control and large part of the off state of the converter.

One switching period is completed. Next another switching period starts and goes on.

III. SS CONDITIONS

In order to achieve SS for the main and the auxiliary switches, the following conditions should be satisfied in the circuit.

A. Main Switch Turn ON With ZVT: While the main switch is in OFF state, the control signal is applied to the auxiliary switch. The parasitic capacitor of the main switch should be discharged completely and the main switch's antiparallel diode should be turned ON. The ON state time of the antiparallel diode is called t_{ZVT} and in this time period, the gate signal of the main switch should be applied. So, the main switch is turned ON under ZVS and ZCS with ZVT.

B. Main Switch Turn OFF With ZCT: While the main switch is in ON state and conducts input current, the control signal of the auxiliary switch is applied. When the resonant starts, the resonant current should be higher than the input current to turn ON antiparallel diode of the main switch. The ON-state time of the antiparallel diode (t_{ZCT}), has to be longer than the main switch's fall time (t_{fS_1}) is in ON state, the gate signal of the main switch should be cut off to provide ZCT for the main switch.

C. Auxiliary Switch Turn ON With ZCS

The auxiliary switch is turned ON with ZCS because the coupling inductance limits the current rise speed. The current pass through the coupling inductance, should be limited to conduct maximum input current at the end of the auxiliary switch rise time (t_{rS_2}). So, the turn-ON process of the auxiliary switch with ZCS is provided.

D. Auxiliary Switch Turn OFF With ZCS: To turn OFF the auxiliary switch with ZCS, while the auxiliary switch is in ON state, the current pass through the switch should fall to zero with a new resonant. Then, the control signal could be cut off. If C_S is neglected, L_{R1} value should be two times more than L_{R2} to fall the auxiliary switch current to zero. Because the current cannot stay at zero as long as the auxiliary switch fall time (t_{fS_2}), the auxiliary switch is turned OFF nearly with ZCS.

IV. DESIGN PROCEDURE

The proposed converter use active snubber circuit for SS. This snubber circuit is mainly based on the ZVT turn-ON and ZCT turn-OFF processes of the main switch. The circuit also provides SS for the other semiconductor components in the converter. For SS of the semiconductors L_{R1}, L_{R2} and C_R ratings should be chosen according to the following features. But, a detailed analysis is not done for the minimization of the additional losses.

i. C_S capacitor is the sum of the parasitic capacitors of the main switch S_1 and the main diode D_F. The value of the current pass through the coupling inductance should be limited to conduct maximum input current at the end of the auxiliary switch rise time (t_{rS_2}). So, L_{R2} value is limited with equation:

$$\frac{V_o}{L_{L_{R2}}} t_{rS_2} \leq I_{imax} \quad (1)$$

ii. In theoretically, the value of L_{R1} should be at least two times more than L_{R2} to turn OFF S_2 with ZCS, if C_S is neglected. This is defined as follows:

$$L_{R1} \geq 2\, L_{R2} \quad (2)$$

However, if C_S is not neglected, this rate can be lowered

iii. To turn OFF S_1 with ZCT, the duration of t_{ZCT} is at least longer than fall time of S_1 (t_{fS_1}). This can be defined as follows:

$$t_{ZCT} \geq t_{fS_1} \quad (3)$$

iv. C_R value is determined by L_{R1}, L_{R2} and C_S to provide t_{ZCT} time both with the greater resonant current than input current, and also to minimize the transient time for PWM.

v. The coupling inductor output turns N_2 should not be determined more than 1–1.5 times of input turns N_1. If this ratio increases, the transferred energy to the output falls and the output voltage stresses increase. N_1 turns can be determined as L_{R2} value. This can be determined as follows:

$$N_1 \leq N_2 \leq 1.5 N_1 \quad (4)$$

VIII. RESULTS

Simulation is done using Matlab Simulink and the results are presented. The circuit shown in Fig.2 has been simulated. The PFC converter is obtained by adding ZVT-ZCT PWM active snubber circuit to the step up converter, which can be fed by universal ac input line. Fig.3 shows the speed and armature current of PMDC motor. Fig.4 shows the input side power factor i.e. before connecting to PFC converter, which is measured as 0.8911. Fig.5 shows the output side power factor i.e. PMDC motor's power factor after connecting PFC converter, which is measured as 0.9999. Fig.6 is the schematic diagram of PFC converter.

SIMULATION CIRCUIT

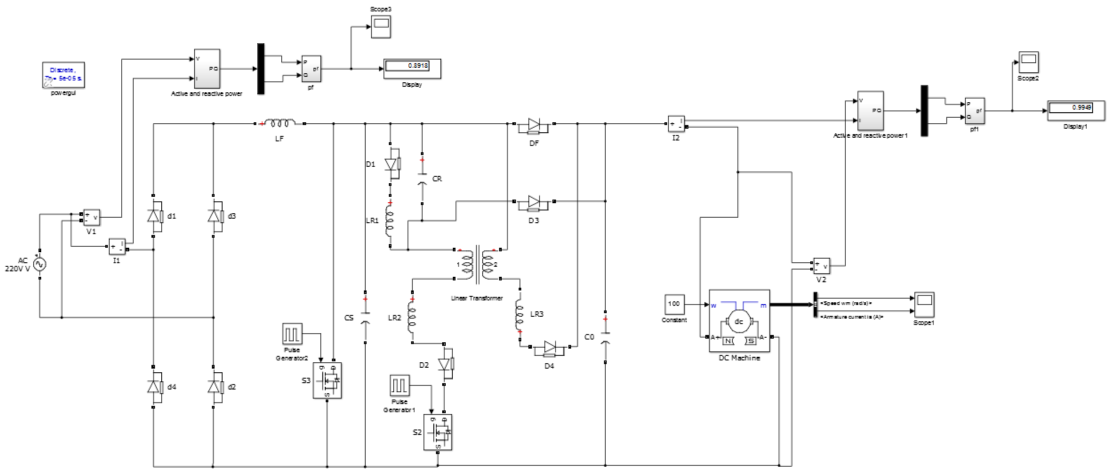

Fig: 2 Simulation circuit diagram of power factor converter for PMDC motor

OUTPUT WAVEFORMS

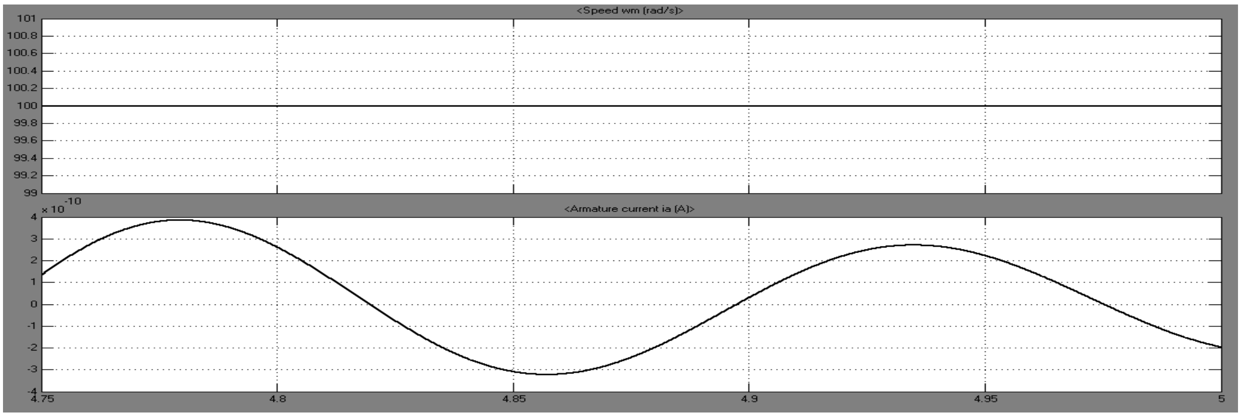

Fig: 3. Motor speed & Armature current

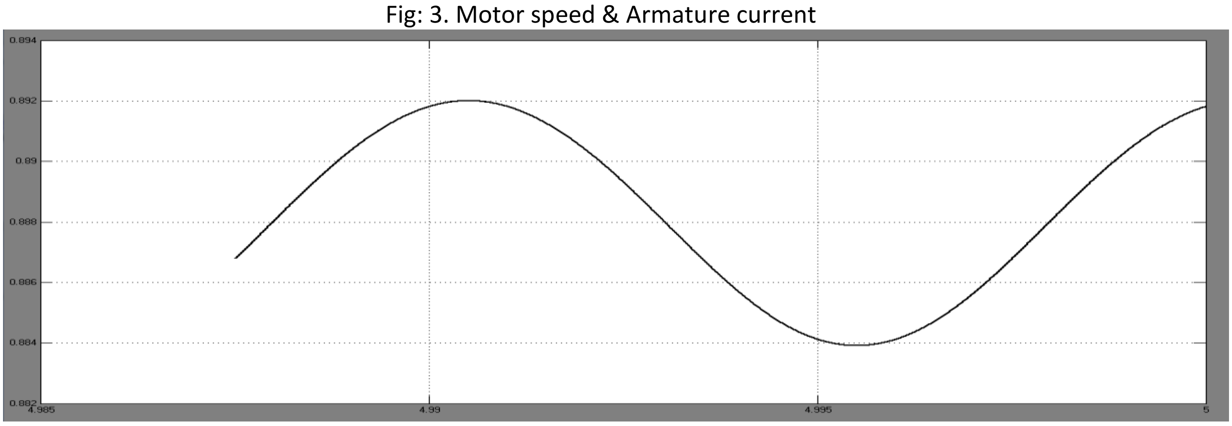

Fig: 4. Input side power factor

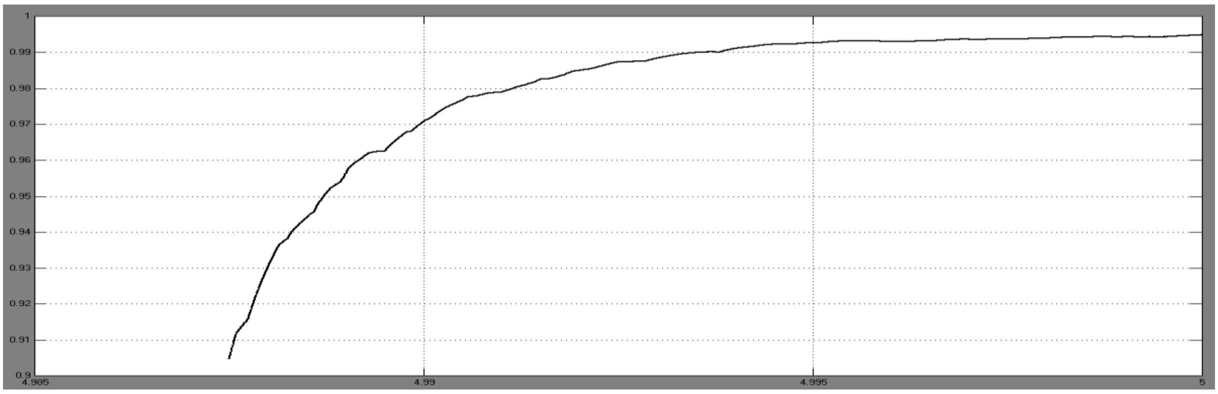

Fig: 5. Output side power factor

PROTEUS SCHEMATIC DIAGRAM

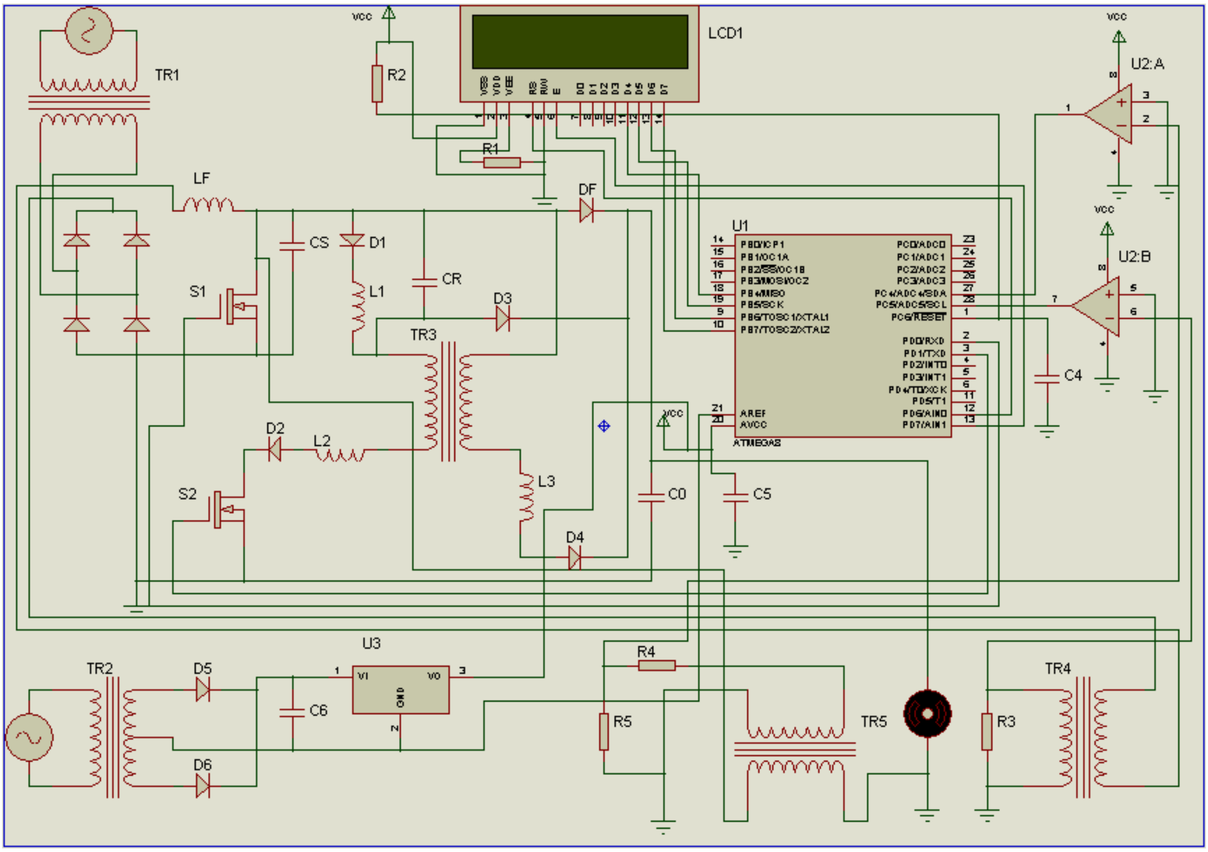

Fig: 6. Proteus Schematic Diagram

CONCLUSIONS

In this study, a new active snubber circuit is used for PFC converters. For this purpose, only one auxiliary switch and one resonant circuit is used. The main switch and all the other semiconductors are switched by ZVT and ZCT techniques. The new active snubber circuit is applied to the boost converter, which is fed by rectified universal input ac line. As a result, the new PFC converter was carried out.

The main switch is turned ON with ZVT and turned OFF with ZCT; the auxiliary switch is turned ON and turned OFF with ZCS. Also, all other semiconductors are switched with SS even at light-load conditions. A part of the current on the auxiliary switch is transferred to the output load by the coupling inductance to improve the efficiency of the converter. The diode is added serially to the auxiliary switch path to prevent the incoming current stresses from the resonant circuit to the main switch. There are absolutely no current or voltage stresses on the main switch. Although, there is no additional voltage stress on the auxiliary switch, the current stress is reduced by transferring this energy to the output load by the coupling inductance. Finally, 99% efficiency at full load is achieved.

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