International Journal of Engineering Research-Online
A Peer Reviewed International Journal
Articles available online http://www.ijoer.in

Vol.3., Issue.6., 2015
(Nov.-Dec.,)

RESEARCH ARTICLE

ISSN: 2321-7758

PERFORMANCE ANALYSIS OF DUAL EDGE TRIGGERED CIRCUITS

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ABSTRACT
Flip flops and latches are important elements in performance contribution of VLSI circuits. Explicit pulse triggered flip-flop which provides high speed operation due to high toggle rate. This project focus on explicit pulsed dual edge triggered sense amplifier flip-flops(DETSAFF) for high performance and low power. In DETSAFF pre-charging technique is implemented and to reduce power further MCGSAFF is developed. In MCGSAFF a new fast latch is embedded for high speed operation at low switching activity. The proposed circuit is simulated in 0.18µm CMOS technology with the power supply of 1.8V and simulations are carried out by using HSPICE tool.

Keywords :Flip-Flops; Sense-amplifier; Clock-gated ..

INTRODUCTION

Flip-Flops are the components which store bits in digital circuit designs. The clock system, consists of the clock distribution network and flip-flop or latches which are more power consuming components in a VLSI system. It scores for 30% to 60% of the total power dissipated in a system where 90% is consumed by flip-flops. The power consumption is proportional to frequency, with reduction in frequency power consumption reduces. In dual edge triggered frequency is reduced to half of frequency when compared with single edge triggered. In dual edge triggered data is sampled on both rise edge and fall edges of the clock. Pulse triggered flip flops have been expressed as an substitute to the conventional master-slave. Pulse triggered flip-flops can be distinguish into two types, implicit-pulsed and explicit-pulsed flip-flops. At half the frequency same throughput is obtained in dual edge triggered flip-flops. Sense Amplifier flip-flop (SAFF) is used in low power and high performance applications. These have different inputs and different with buffered outputs. SAFF consists of two stage, i. e. , sense amplifier and R-S latch. The first stage senses true and complementary inputs. Second stage captures and hold the transitions until the next active clock edge arrives.

This paper is organized as follows: section II review of designs related to the proposed work. Section III discusses the proposed technique Section IV Simulation results V wind up the paper.

REVIEW OF DESIGNS RELATED TO PROPOSED WORK

Static Ouptut-Controlled Discharge flip-flop

In Static Output-Controlled Discharge flip-flop(SCDFF) a pulse is generated from pulse generator and is given to static latch circuit. The schematic is shown in figure1. At rising and falling edges transmission gates TG1 and TG2 are activated in consequence, a pulse is created. In static latch circuit which is operated in two stages, when D is high Q assumed to low so that X is discharged though M2, M3, M4 pulling Q to high. This is sampling period. When D is low M7 is on through which Q is discharged. A delay is presented between Q and QB due to single ended nature of SCDFF.

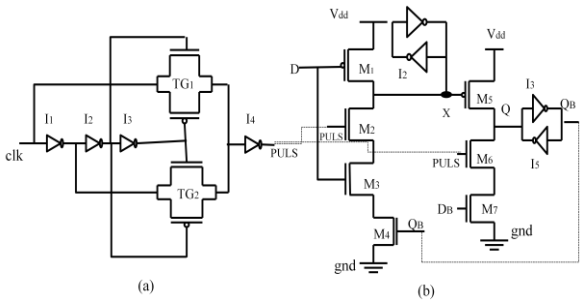


Figure. 1 (a) Pulse Generator (b)static latch

Dual Edge Triggered Static-pulsed flip flop

Dual-edge triggered static pulsed flip-flop(DSPFF) has pulse generation circuit and static latch circuit. In pulse generator, pulse is generated at both transition edges of clock. Delay signals are generated using four inverters. These signals with two nMOS pass transistors generates pulse signal. In static latch, pulse generated is given to N1 and N2 pass transistors which are turned on. When N1 and N2 are on input data is captured so that SB or RB will be discharged.

SB and RB are directly fed from D and DB so that small delay is obtained. When flip-flop is opaque pMOS transistor with weak nmos transistors avoid floating nodes of SB and RB. A high voltage drop across N3 or N4 causes high leakage current when they are off.

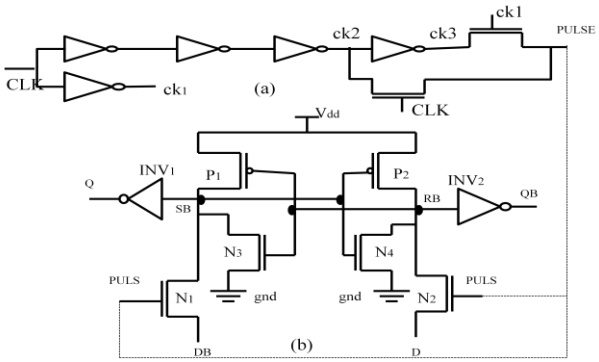


Figure. 2 (a) Pulse Generator (b) Static Latch

Adaptive Clocking Dual Edge Triggered Sense-Amplifier Flip-Flop

The schematic of Adaptive Clocking Dual Edge Triggered Sense-Amplifier is shown in figure. It consists of adaptive clocking inverter chain, sensing stage and a modified latch called Nikolic's latch. Some internal clocked transistors are disabled when data activity is low. A signal NC is derived from sensing stage. When D is different from Q, NC is pulled to high. Due to this N1 and N2 are on generating CLK3 and CLK4 so that a narrow transperant signal is created at rising and falling edges. The output state changes when CLK3 and CLK4 are produced because SB or RB are discharged during this period.

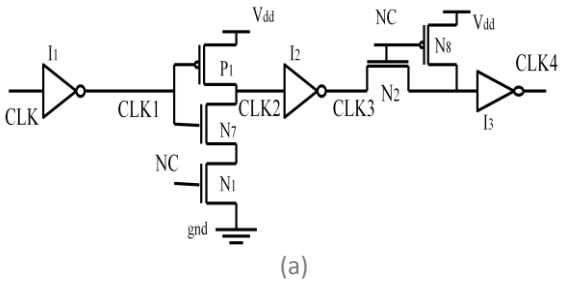


Figure. 3 (a) adaptive clocking inverter chain

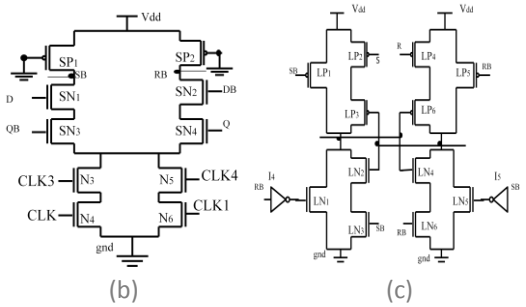


Figure. 3 (b)front end sensing stage (c) Nikolic's latch

When output is changed, inverter chain is disabled as NC is blocked or discharged either through N3 and N4 or N5 and N6. When D is same as Q, flip-flop is opaque. Due to more transistors more power is consumed and circuit is complex.

Dual Edge Triggered Sense-Amplifier Flip-Flop

The Schematic diagram of Dual Edge Triggered Sense-Amplifier Flip-Flop is shown in figure. Dual Edge Triggered Sense-Amplifier Flip-Flop consists of pulse generating stage, sensing stage and symmetric latch which is modification of latching stage. In pulse generator, at rising and falling edges a narrow transparent pulse is generated by turning on transmission gate and CP3 transistor respectively. In sensing stage, SB , RB are connected to DB and D respectively. When D is low, SB is set to high, if D is high RB is high. By precharging the nodes SB and RB which is conditional precharging technique redundant transistions are eliminated at major nodes. Two pMOS transistors SP1 and SP2 are precharging paths.

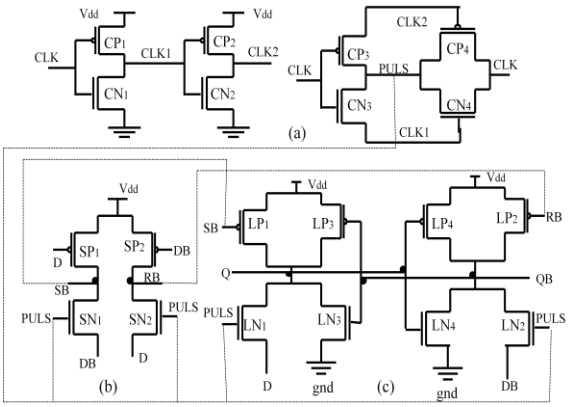


Figure. 4(a)Dual Pulse Generator (b)Sensing stage (c)Symmetric Latch

In latching stage, Nikolic latch is modified to symmetric latch. Output nodes are pulled up by SB and RB. D and DB are directly fed to Q and QB. When pulse is generated, output captures input which speeds-up high-to-low transition. On the other hand, output node is charged by LP1 and LP2 and also through pass transistors LN1 and LN2. This improves the low-to-high latency. At high switching activity, i. e. , α>0. 5, when there is no change in output pulse generator operates, this causes unnecessary transitions and hence consuming more power.

Clock-Gated Sense-Amplifier Flip-Flop

In order to eliminate unnecessary transitions CG-SAFF is developed. A clock gating is implemented in pulse generator to disable transitions which are not needed. Comparators are used to compare previous and current input values, X and Y signals are generated by using differential inputs and buffered outputs. If D is different from Q1(Q), X is pulled to high and Y becomes zero. CN3 is on and CL is produced which is gated clock. When Y is high CP1 is high which drives CLK1 signal to high before rising edge and at this edge CL high, CLK3 remains low. Therefore CN5 and transmission gate are on which generates pulse at low to high transition. After this transition CLK1 goes low and CLK3 to high. Thus a pulse is generated at rising edge. At falling edge, CL low and CLK3 high and thus CP5 is high which drives the pulse to high at high to low transitions. If there is no change in input for consecutive cycles X is low and Y to high. When Y is high CN4 is on CL is pulled down by this and CLK3 will be low irrelevant of CLK. As a result flip-flop is opaque and thus power can be saved.

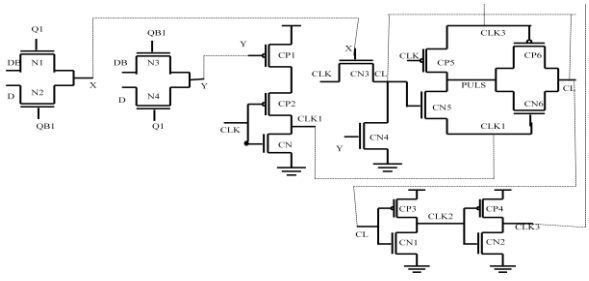


Figure. 5(a) Clock Gated Pulse Generator

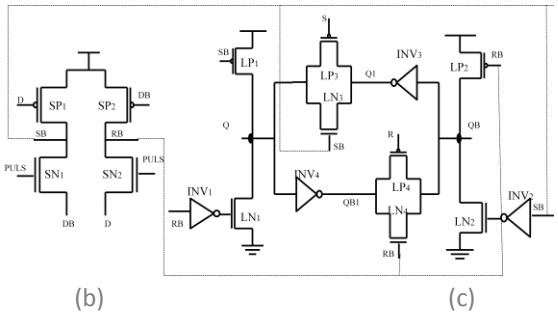


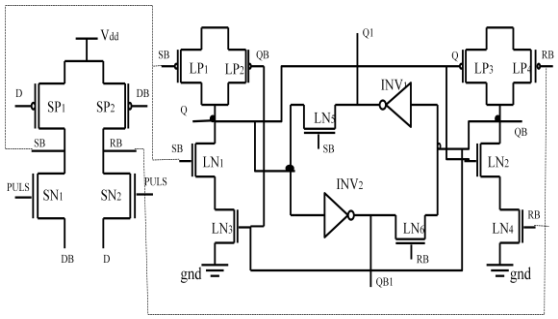
Figure. 5(b)Sensing Stage (b) Latching Stage

The sensing stage is same as DET-SAFF. The latching stage is modified because pulse is heavily loaded. It provides stable operation because it does not require any clock signal. Buffered outputs are obtained by modifying latch. Instead of Q and QB, Q1 and QB1 are used to generate X and Y which improves performance.

PROPOSED TECHNIQUE

Modified Clock Gated Sense-Amplifier Flip-Flop

In Modified Clock Gated Sense-Amplifier Flip-Flop latching stage is modified to reduce power and increases performance at low to high transition. It consists of three different stages , i. e. , clock gated pulse generator, sensing stage and latching stage.



(b) (c)

Figure. 6 (b) Sensing Stage (c) Modified Latching Stage

In pulse generator stage, clock gated signal CL is high at rising edge and discharges at falling edge through CN4 due to this signal unnecessary transitions are eliminated. CL, CLK3 are high at high to low transition and CL, CLK4 at high to low transition. Sensing stage is same as CG-SAFF. The latching stage is modified. If D is high RB set to high and SB to low driving LP1 which pull up node Q and LN4 is high which acts as pull down path. This speed up the operation at low to high transition because output captures input when pulse is generated.

SIMULATION RESULTS

In this paper, different dual edge triggered flipflop designs are simulated using HSPICE 0. 18µm technology library at 27°C temperature and 1. 8V voltage. Modified clock gated flip-flop design performance is evaluated by comparing with previous dual edge triggered flip-flop designs.

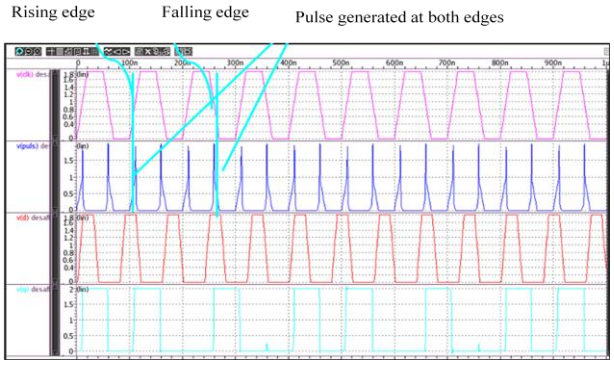


Figure. 7 waveform of Dual Edge triggered Sense-Amplifier

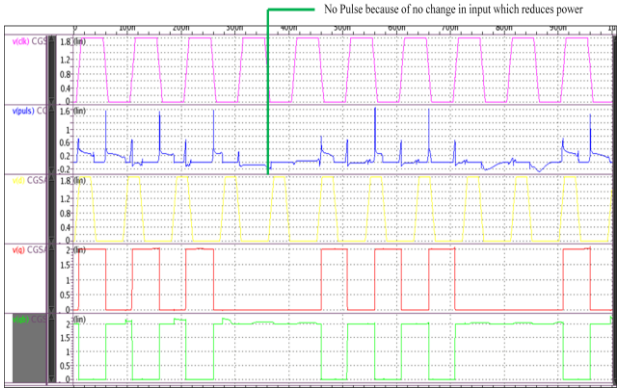


Figure. 8 Waveform of Modified Clock Gated Sense-Amplifier

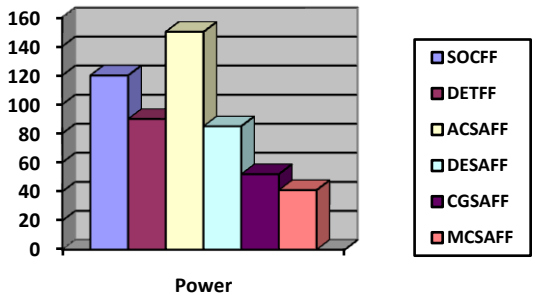


Figure. 9 Power Consumption for different Designs

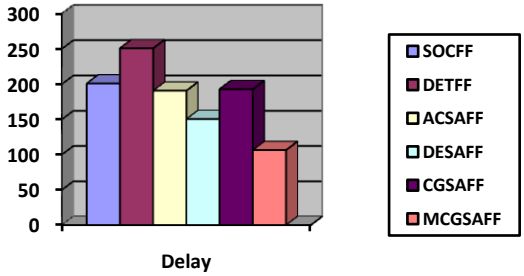


Figure. 10 Delay for different Designs

Table. 1 PDP at different Switching activity

Designs	DETSAFF	CGSAFF	MCGSAFF
PDP(α=1)	90. 35	105. 49	78. 21
PDP(α=0. 5)	69. 78	83. 25	57. 75
PDP(α=0)	50. 28	70. 58	45. 25

The above table gives information of Power Delay product for different switching activities. When switching activity reduces PDP also reduces.

CONCLUSION

The Dual edge triggered sense amplifier circuits are outlined. Using dual edge circuit, performance is increased by modifying latch stage of the circuit. Switching activity is varied and power-delay product is calculated. The PDP for MCGSAFF is reduced compared to CGSAFF and DETSAFF.

Acknowledgment

I express my profound sense of gratitude to my guide K. Rajasekhar, Assistant professor, JNTU Kakinada for his systematic guidance and valuable advices. I would like to express my sincere gratitude to Dr. A. M. Prasad, professor, Head of the department and Dr. K. Babulu, professor, course coordinator, for providing me with all the necessary facilities for the work.

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