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# PERFORMANCE ANALYSIS OF AN 8-BIT PIPELINED RISC PROCESSOR

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**ABSTRACT**
In the present work, the performance analysis of an 8 bit pipelined RISC processor is done. Pipelining allow the processor to handle several instructions at the same time. The processor can work at a high clock frequency and thus yields higher speed. This paper is about comparing and analyzing the unpipelined processor and pipelined processor performances. Program codes are written in Verilog HDL. Simulations are done using ModelSim.
Keywords: RISC, Pipelining, Verilog HDL, ModelSim.



**INTRODUCTION:**

The Processor is a programmable device that takes in numbers, performs on them arithmetic or logical operations according to the program stored in memory and then produces other numbers as a Result. Processor is also an electronic circuit that functions as the central processing unit (CPU) of a computer, providing computational control. Computers are common and important tools for everyday activities. With the simple design technology and the decreasing cost of the integrated circuit, RISC processor is increasing widely used in every field. The simple design provides higher performance, cost-effective, compatible systems. Some typical applications include: data processing, scientific and engineering applications and real-time control.

**II.RISC features:**

The RISC Processor works on (features are) reduced number of Instructions, Simple operations, only load and store operations access memory and Rest of the operations on a register-to-register basis, Pipelined, Simple uniform instructions, fixed instruction length, No microcode, Many identical general purpose registers, load-store architecture and simplified addressing modes which makes individual instructions execute faster, achieve a net gain in performance and an overall simpler design. RISC architecture starts with a small set of most frequently used instructions which determine the pipeline structure of the machine enabling fast execution of those instructions in one cycle.

**III.UNPIPELINED PROCESSOR**:

Unpipelined processor executes each instruction in one clock cycle. Values stored in one clock edge flow through the date path and the machine is updated on the next clock edge. The clock period must be long enough for the slowest path through the design. An unpipelined processor executes only one instruction at a time. So, only one instruction can be working at a time. The figure given below shows the block diagram of an unpipelined processor. This shows how an instruction flows through a data path. At the end of each clock cycle every value computed during a clock cycle and required on a later clock cycle is written into a storage device which may be mem, GPR and temporary register. The temporary register holds value between clock cycles for one instruction.

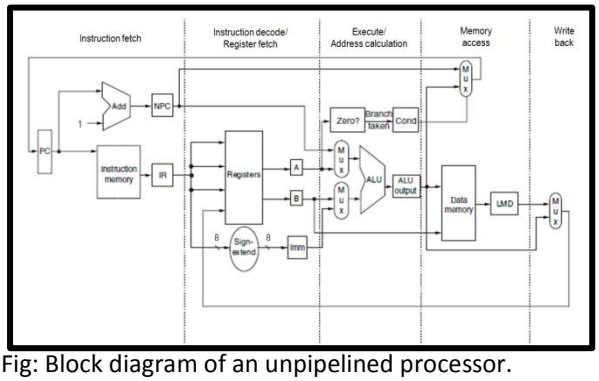


Fig: Block diagram of an unpipelined processor.

**IV.PIPELINED PROCESSOR:**

Pipelining, a standard feature, is an implementation technique used to improve both CPI (Cycle per Instruction) and overall system performance. Pipelining allows a processor to work on different steps of the instruction at the same time, thus more instruction can be executed in a shorter period of time. The sole purpose of many of those features is to support an efficient execution of RISC pipeline.

Every pipe stage is active on every clock cycle, all operations in a pipe stage must complete one clock cycle and combination of operations must be able to occur at once. Furthermore, pipelining the data path requires that values passed from one pipe stage to the next must be placed in registers. All the registers needed to hold values temporarily between clock cycles within one register (IR);which is part of the IF/ID register. The pipeline registers carry both data control from one pipeline stage to the next. Any value needed on a later pipeline stage must be placed in such register and copied from one pipeline register to the next. The figure given below shows the bock diagram of a pipelined processor.

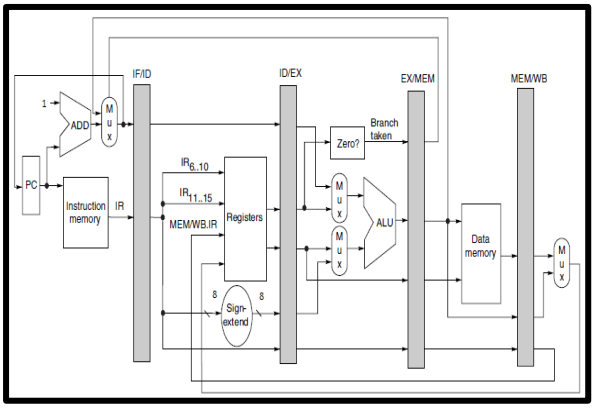


Fig: Block diagram of a pipelined processor.

**III.IMPLEMENTATION:**

The code is written for both pipelined and unpipelined processor using Verilog HDL. Verilog standardized as IEEE 1364, is a Hardware Description Language (HDL) used to model electronic systems. It is most commonly used in design and verification of digital circuits. It is also used in verification of analog circuits and mixed signal circuits. Verilog HDL has evolved as a standard hardware description language. By using HDL one can describe any hardware at any level. HDLs allows design to be simulated earlier in design cycle in order to correct errors on experiment with different architectures. Design described in HDL are technology independent , easy to design and debug. Verilog is capable of describing simple behavior .The simulations are done using the ModelSim tool. Modelsim is a multilanguage HDL , for simulation of Hardware description language such as VHDL Verilog etc. Modelsim offered in multiple editions such as ModelSim SE, ModelSim PE , ModelSim XE .ModelSim SE offers high performance and advanced debugging capabilities. ModelSim SE is used in large multi-million gate design and is supported on microsoft windows and Linux , in 32 bit and 64 bit architectures.

**IV.SIMULATION AND RESULTS:**

Waveforms for an unpipelined processor:

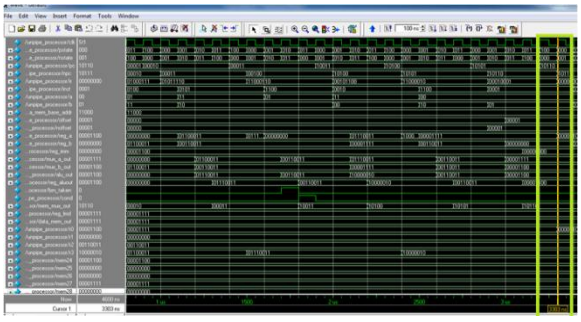

Table showing performance parameters calculated for an unpipelined processor:

| PARAMETERS | UNPIPELINED IMPLEMENTATION |
|---|---|
| Number of instructions | 7 |
| Clock cycles | 33 |
| CPI | 4.7 |
| CPU Time | 3290ns |

Waveforms for a pipelined processor:

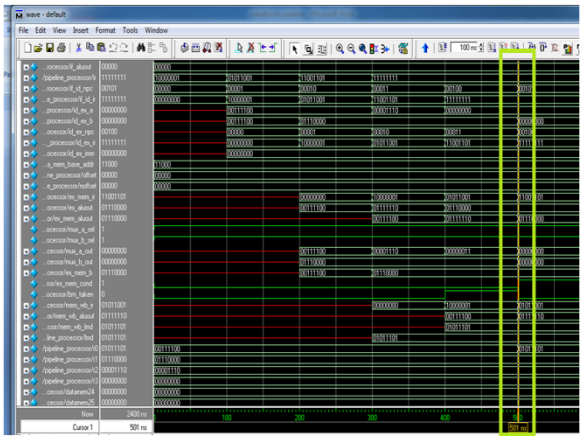

Table showing performance parameters of a pipelined processor:

| PARAMETERS | PIPELINED IMPLEMENTATION |
|---|---|
| Number of instructions | 7 |
| Clock cycles | 14 |
| CPI | 2 |
| CPU Time | 1400ns |

**V. CONCLUSION:**

This paper shows the implementation of both an unpipelined processor as well as a pipelined processor. The performance parameters like clock cycles required, CPI, and CPU Time have been calculated for both the processor designs and it has been clear from the simulation results that the pipelined processor yields a higher performance as compared to an unpipelined processor.

**VI. ACKNOLEDGEMENT:**

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