



DESIGN AND SIMULATION OF SOLID STATE POWER AMPLIFIER AT 400MHZ FOR RADAR APPLICATIONS

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ABSTRACT

This paper proposes a designing and simulation of Solid State Power Amplifier (SSPA) by using Advanced Design System (ADS) software which is useful for radar applications. The selection of proper device for the suitable application is a main thing. There are different steps involved in the present design such as Direct Current (DC) simulation in order to obtain the proper operating point under the platform. Afterwards Stability factor simulation is to be carried out to confirm that the amplifier can be unconditionally stable. Load pull simulation and Source pull simulation are required to match the load impedance and source impedance, and finally Harmonic Balance (HB) simulation is to be carried out to verify the harmonic levels of the signals other than the designed frequency of operation.

KEYWORDS: Solid State Power Amplifier (SSPA), Power Amplifier (PA), Advanced Design System (ADS), Direct Current (DC) and Harmonic Balance (HB).

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I. INTRODUCTION

The main specifications while designing an amplifier are 10MHz bandwidth, 17% efficiency, 30dB output power, reliability, better thermal performance and 11dB gain of the amplifier. A main object in Radio Frequency (RF) front end is the Power Amplifier (PA). The main specifications for Power Amplifier design include linearity and output power. Linearity must be maximized in order to reduce signal distortion and minimize Adjacent Channel Leakage Ratio (ACLR). This paper describes the process of designing a single stage class AB Power Amplifier for operation at the 400MHz frequency.

II. NEED OF A POWER AMPLIFIER

Power Amplifier is the major part in the transmitting chain of radar system and it is the final amplification stage before the signal is transmitted. So it must produce the high output power to overcome channel losses between the transmitter and receiver.

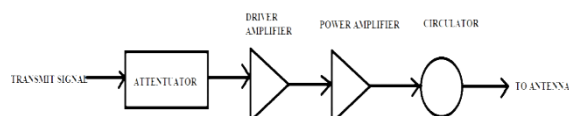


Fig 1. Transmission path of T-R Module

III. EXISTED SYSTEM

The existed Power Amplifier for radar application is Klystron amplifier. Solid State Power Amplifier have more reliability than klystron amplifier. Klystron amplifier requires high power supplies and its life span is very low compared with the SSPA. The mean time between the failures is low in Klystron amplifier. To overcome the above problems here we are going to design the Solid State Power Amplifier.

IV. SOLID STATE POWER AMPLIFIER

An amplifier that uses transistor (BJT or FET) to get useful amplification at Mega or Giga hertz frequencies. Power Amplifier is an important part of modern wireless system. The main purpose of an amplifier is to take an input signal and make it stronger. Not all the power amplifiers are same and there is a difference between the way of their output stages are operate. The most important operating characteristics of an ideal amplifier are linearity, signal gain, efficiency and output power.

V. CLASSIFICATION OF SOLID STATE POWER AMPLIFIERS

The PA is classified into different classes based on the operating point of the circuit. Power Amplifiers are mainly classified into two types amplifier and Nonlinear amplifier, this can be divided based on linearity, efficiency and circuit topologies. Class A, Class B and Class AB are linear amplifiers. Class A has the highest linearity. Nonlinear amplifier classes are Class C, D, E, F, G and H. Here we are going to design a class AB amplifier because it has more efficiency than class A and it reduces the cross over distortion, which is present in class B. Linearity is also the important criteria in the selection of Power Amplifier for radar applications. But in radar applications the efficiency is not a major criterion. So we can also use class A amplifier. But the class A amplifier has a major disadvantage i.e., the transistor is on during both the cycles. Due to this the power dissipation is observed continuously which spoil the Power Amplifier circuit. But this is not observed in class AB amplifier.

VI. CLASS AB POWER AMPLIFIER

A class AB amplifier is a linear amplifier, which is compromise between both class A and class B regarding to efficiency and linearity parameters and operates between two edges defined for these

two amplifiers. For ideal case, an operating class AB mode is biased to a quiescent point, which is in the region between the cutoff point and the bias point of class A. Efficiency is improved compared to class A PA, but still less than 78.5% by virtue of conduction angle in this class is between 180° and 360° . Unlike class B amplifier, the conduction angle for a class AB amplifier being a function of drive level results in distortion of amplitude modulated signals at their peak power level.

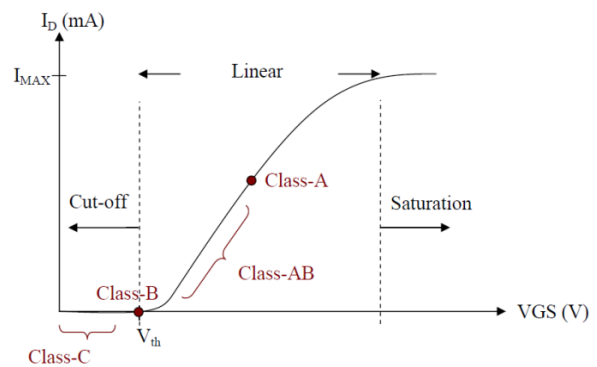


Fig 2. Transfer Characteristics of FET

VII. INTRODUCTION TO ADS

Advanced design system (ADS) is an electronic design automation software for Radio Frequency, microwave and high speed digital applications. It is powerful and easy to use interface. It contains so many bundles like passive components active components micro strobes, including PLL (phase locked loops) design, time domain and EM modeling. Advanced design system break new ground to the most innovative and commercially successful technologies. To design a power amplifier the following steps are required.

VIII. DESIGNING STEPS AND SIMULATION RESULTS OF A POWER AMPLIFIER

1. DC and Load line Analysis
2. Bias and Stability Analysis
3. Load pull Analysis
4. Harmonic Balance Simulation

TYPE OF TRANSISTOR USED IN THIS DESIGN

Selection of the transistor is main thing in power amplifier design. The transistor is selected as per our requirement. Here I used MRF134 transistor for designing PA at 400 Mhz frequency. The transistor can be used up to 400 Mhz.

1. DC LOADLINE ANALYSIS

DC simulation is doing for finding the bias or operating point. After simulation we will get the transistor characteristics and add below equations in the result then we get DC load line with that we can

select the operating point. And finally we can classified the classes of power amplifier. For DC simulation first we should select the FET curve tracer from schematic design templates, add selected transistor with proper connections and simulate it.

$$\text{Eqn slope} = \frac{m_3 - m_2}{i(\text{indep}(m_3) - \text{indep}(m_2))}$$

$$\text{Eqn C} = m_2 - \text{slope} * \text{indep}(m_2)$$

$$\text{Eqnload_line} = \text{slope} * \text{VDS}[0..:] + c$$

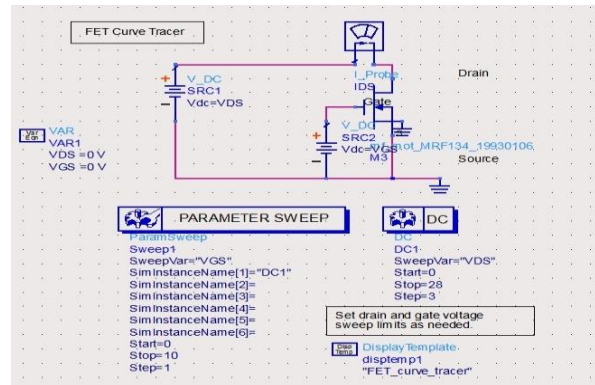


Fig 3. FET Curve Tracer circuit in ADS

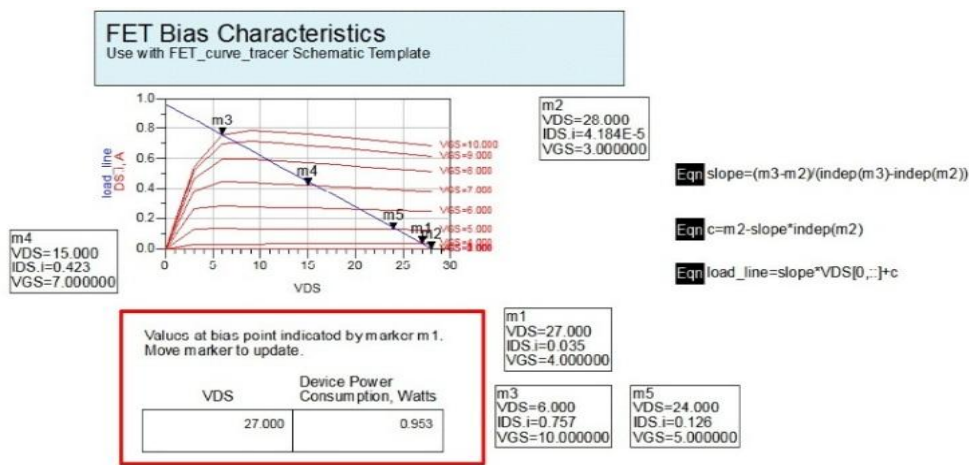


Fig 4. FET Curve Tracer simulation in ADS

1. BIAS AND STABILITY ANALYSIS

Bias and stability analysis is doing for finding stability factor. Here we will get the stability factor by using S-parameter simulation. We have Different types of biasing techniques but as per our requirement potential divider bias is suitable. Below shows the circuit that was adding potential divider. We should get the stability factor less than or nearly equal to 1. We must add stab fact in the design to get stability factor

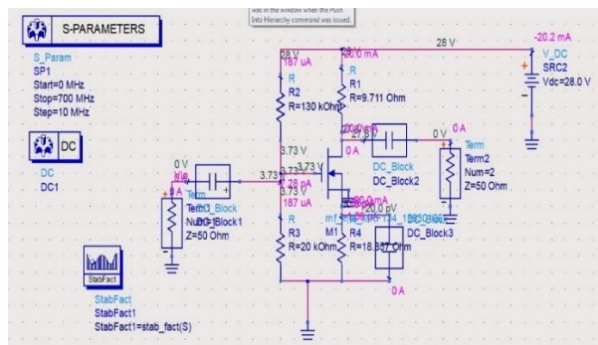


Fig 5. Bias and Stability circuit of FET in ADS

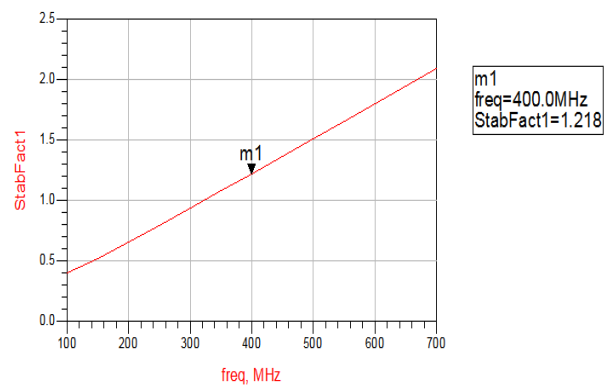


Fig 6. Bias and Stability circuit simulation of FET MRF134 in ADS

2. LOADPULL SIMULATION

Load pull simulation is widely used in RF power amplifier design and characteristics. In a load pull simulation range of load impedance are represented to the power amplifier output power and power added efficiency (PAE) measured for load impedance. The results are plotted on smith chart.

Load pull simulation uses the built-in ADS one tone load-pull circuit simulator. Different values of load impedance are applied to find the optimum one, which meets the required value of gain, output power and efficiency. Before running the simulation, some parameters like frequency, V_high and V_low have to be set.

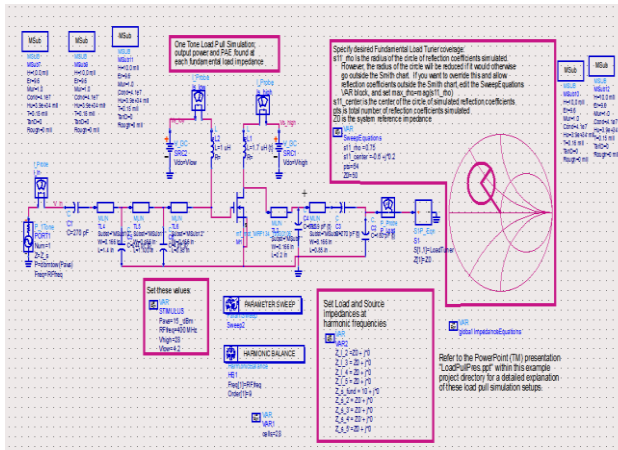


Fig 7. Load pull circuit of FET MRF134 in ADS

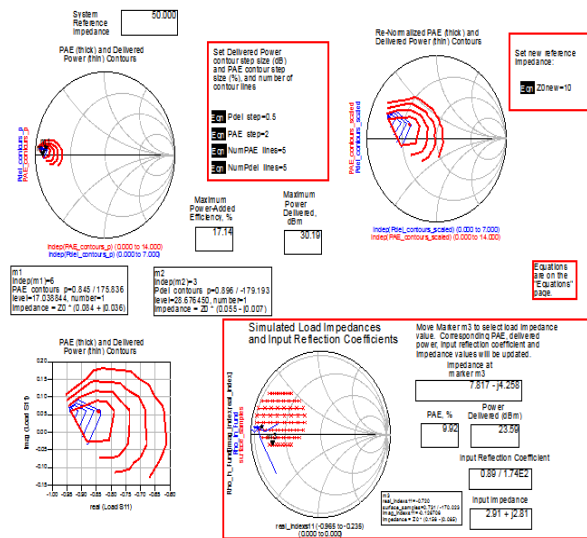


Fig 8. Load pull circuit simulation of FET MRF134 in ADS

3. HARMONIC BALANCE SIMULATION

The performance of the design based on the output power and the efficiency, one tone harmonic balance simulation must be done. The harmonic balance simulation circuit is designed by using the above all resulting circuits. Add bias and stability circuit and load pull circuit into a single circuit then we get the result of harmonic balance simulation. The Harmonic Balance circuit is shown below.

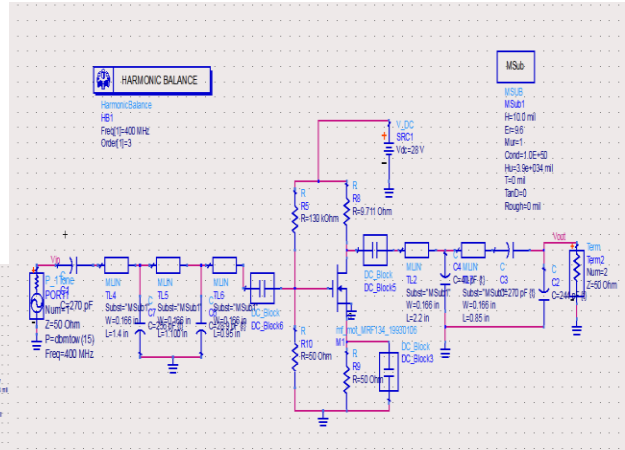


Fig 9. Harmonic Balance circuit of FET MRF134 in ADS

m1 freq=400.0MHz dBm(Vout)=-26.393	m2 freq=800.0MHz dBm(Vout)=-71.220	m3 freq=1.200GHz dBm(Vout)=-101.007
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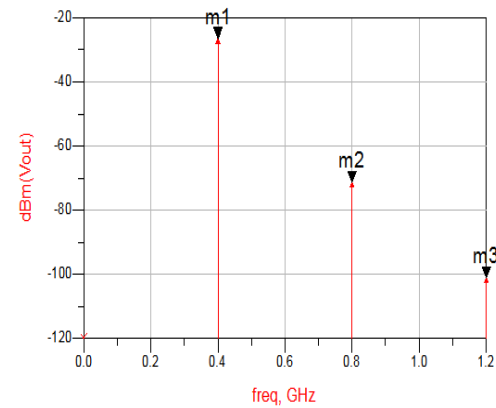


Fig 10. Harmonic Balance circuit simulation of FET MRF134 in ADS

CONCLUSION

This paper proposes design of Solid State Power Amplifier for radar applications using ADS software. here I have designed an amplifier I got the desired results in all simulation but load pull simulation has the little bit issue. I didn't get the exact efficiency as per requirement.

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