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RESEARCH ARTICLE

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PERFORMANCE ENHANCEMENT BY DEADBEAT CURRENT CONTROL SYSTEM FOR GRID CONNECTED INVERTER WITH LLCL FILTER

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ABSTRACT

A higher order power filter (LLCL filter) for the grid-tied inverter is becoming attractive for industrial applications due to the possibility to reduce the cost of the copper and the magnetic material. However, similar to the conventional LCL filter, the grid-tied inverter is facing control challenges. An active or a passive damping measure can be adopted to suppress the possible resonances between the grid and the inverter. For an application with a stiff grid, a active damping method is often preferred for its simpleness and low cost. This paper introduces a new active damping scheme with low power loss for the LLCL filter. Also, a simple engineering design criterion is proposed to find the optimized damping resistor value, which is both effective for the LCL filter and the LLCL filter. It is concluded that, compared with the LCL filter, the proposed passive damped LLCL filter can not only save the total filter inductance and reduce the volume of the filter but also reduce the damping power losses for a stiff grid application.

Key Words: Grid connected inverter, LLCL filter, PWM, grid and inverter current feedbacks, DEADBEAT current control system etc

I. INTRODUCTION

Since renewable energy generation is gaining more and more attention, the grid-tied inverter has been widely adopted [1]–[3]. A low-pass power filter is often inserted between a voltage-source inverter (VSI) and the grid to limit the excessive current harmonics, which are most often caused by the sine pulsewidth modulation (PWM), to inject into the pointof connection. Due to the increasing price of copper, many measures have been adopted to cut down the cost of the power filter. One effective way is to raise the switching frequency of the inverter where the solution certainly depends on the device techniques and costs. For example, an SiC device can switch with a much higher frequency than the same power ratio silicon device does, but with a much higher price.

Another measure focuses on special topologies or controls. In [4] a dual mode time-sharing inverter was introduced, trying to utilize the good performance of the low-voltage device to achieve higher switching frequency. In [5] and [6] dual-mode time-sharing control methods for single- and three-phase inverters, respectively, was proposed to maximize the modulation index and reduce the output power filter size. However, it makes the topologies or controls much more complex, leading to loss of reliability. Furthermore, it is very difficult for a dual-mode timesharing type inverter to compensate the harmonics or generate reactive power for the grid.

The most common solution is to use a Higher-order *LLCL* filter instead of a first-order *L* filter [7]. Compared with the firstorder *L* filter, the *LLCL* filter can meet the grid interconnection standards with significantly smaller size and cost, especially for applications above several kilowatts, but it might be more difficult to keep the system stable [8]–[10]. Moreover, selecting the parameters of an *LLCL* filter is also a more complicated process in contrast to an *L* filter [11], [12]. Sometimes, it is difficult to balance the factors of output current ripple sourced by insulated gate bipolar transistor switches, fundamental voltage drop, volt ampere reactive limits, and the resonance frequency.

The schematic diagram of the grid-side inverterconnected to the grid via an LLCL filter
is shown in fig.1.

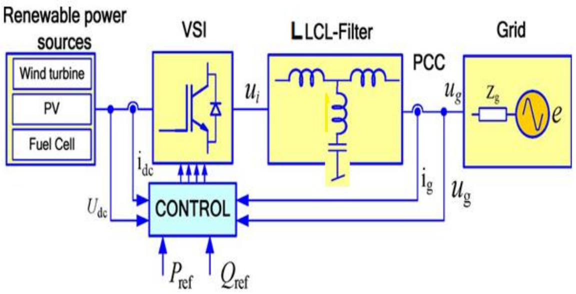


Fig.1 grid-side inverter as a front end with LLCL filter

In this paper, a new high-order filter, named the *LLCL* filter, is proposed. Based on the traditional *LCL* filter, a small inductor is inserted in the branch loop of the capacitor, composing a series resonant circuit at the switching frequency. It can particularly attenuate the switching-frequency current ripple components much better than the *LCL* filter, saves the total inductance and thereby leads to size reduction.

II. DEADBEAT CURRENT CONTROL

A. Circuit description in α-β stationary frame

The differential equations of the three-phase voltages and currents are defined by:

$$L_1\frac{d}{dt}\begin{bmatrix} i_{1u} \\ i_{1v} \\ i_{1w} \end{bmatrix} = \begin{bmatrix} v_{1u} \\ v_{1v} \\ v_{1w} \end{bmatrix} - \begin{bmatrix} v_{cu} \\ v_{cv} \\ v_{cw} \end{bmatrix} \cdots\cdots\cdots\cdots (1)$$

$$L_2\frac{d}{dt}\begin{bmatrix} i_{2u} \\ i_{2v} \\ i_{2w} \end{bmatrix} = \begin{bmatrix} v_{cu} \\ v_{cv} \\ v_{cw} \end{bmatrix} - \begin{bmatrix} v_{2u} \\ v_{2v} \\ v_{2w} \end{bmatrix} \cdots\cdots\cdots\cdots (2)$$

$$L_f\frac{d}{dt}\begin{bmatrix} i_{3u} \\ i_{3v} \\ i_{3w} \end{bmatrix} = \begin{bmatrix} v_{1u} \\ v_{1v} \\ v_{1w} \end{bmatrix} - \begin{bmatrix} v_{2u} \\ v_{2v} \\ v_{2w} \end{bmatrix} \cdots\cdots\cdots\cdots (3)$$

$$C_f\frac{d}{dt}\begin{bmatrix} V_{cu} \\ V_{cv} \\ V_{cw} \end{bmatrix} = \begin{bmatrix} i_{1u} \\ i_{1v} \\ i_{1w} \end{bmatrix} - \begin{bmatrix} i_{2u} \\ i_{2v} \\ i_{2w} \end{bmatrix} \cdots\cdots\cdots\cdots (4)$$

The variables of a three phase systems defined in (1), (2), (3), can be described as an equivalent two-phase system denoted as α and β using the following transformation matrix:

$$\sqrt{\frac{2}{3}}\begin{bmatrix} 1 & e^{\frac{j2}{3\pi}} & e^{\frac{-j2}{3\pi}} \end{bmatrix} \ldots\ldots\ldots\ldots\ldots\ldots\ldots (5)$$

Using the transformation matrix of (5), the three-phase two-phase transformation of (1) is given by:

$$L_1\sqrt{\frac{2}{3}}\frac{d}{dt}\left(i_{1u} + i_{1v}e^{\frac{j2}{3\pi}} + i_{1w}e^{\frac{-j2}{3\pi}}\right)$$

$$= \sqrt{\frac{2}{3}}\frac{d}{dt}\left(v_{1u} + v_{1v}e^{\frac{j2}{3\pi}} + v_{1w}e^{\frac{-j2}{3\pi}}\right) -$$

$$\sqrt{\frac{2}{3}}\frac{d}{dt}\left(v_{cu} + v_{cv}e^{\frac{j2}{3\pi}} + v_{cw}e^{\frac{-j2}{3\pi}}\right) \text{------} (6)$$

Therefore, the instantaneous space vector equation of (1) described in the α-β stationary co-ordinate frame is defined as follows:

$$L_1\frac{d}{dt}i_1 = v_1 - v_c ------ (7)$$

Similarly, the instantaneous space vector equations of (2) and (3) are represented by

$$L_2\frac{d}{dt}i_2 = v_c - v_2 \text{----------------} (8)$$

$$L_3\frac{d}{dt} = v_1 - v_2 \text{------------------} (9)$$

$$C\frac{d}{dt}v_c = i_1 - i_2 ----- (10)$$

From (7), (8), (9), (10) the space vector equation of the LLCL filter described in the stationary α-β co-ordinate frame can be represented by:

$$\begin{bmatrix} 0 & 0 & -1/L_1 \\ 0 & 0 & -1/L_2 \\ 0 & 0 & 0 \\ \frac{1}{C} & \frac{-1}{c} & 0 \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ v_c \end{bmatrix} + \begin{bmatrix} 1/L_1 \\ 0 \\ 1/L_f \\ 0 \end{bmatrix} V_1 + \begin{bmatrix} 0 \\ -1/L_2 \\ -1/L_f \\ 0 \end{bmatrix} V_2$$

B. Resonant frequency

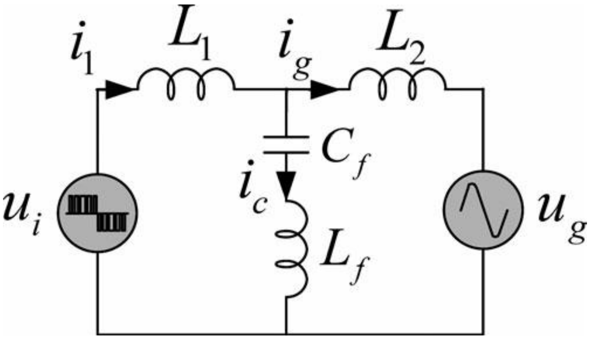


Fig.2 schematic diagram of the LLCL filter

At resonance $X_L = X_C$

$$\frac{1}{\omega L_1} + \frac{1}{\omega L_2} + \frac{1}{\omega L_f} = \omega C_f$$

$$\omega = \frac{1}{\sqrt{\left(\frac{L_1 L_2}{L_1 + L_2} + L_f\right) C_f}}$$

when $f_r \leq 0.5 f_s$ the resonance will be damped.

where f_s = sampling frequency.

III. PARAMETER DESIGN OF THE LLCL FILTER

When designing the power filters(LCL or LLCL) Some limits on the parameter values should be introduced.

(1) The capacitor value C_f is limited to the decrease of the capacitive reactive power at rated load to less than 5%.

(2) The upper limit to the total inductance (L_1+L_2) depends on the voltage drop during operation (lower than 10%).

(3) The value of the inverter-side inductor L_1 is limited to the requirement of the ripple current.

(4) The resonance frequency should be one half of the switching frequency in order to not create resonance problems.

IV. COMPARISON OF LLCL AND LCL FILTERS

LLCL filter can attenuate the switching frequency ripple-components much better than LCL filter. The value of the Grid-side inductor of the LLCL filter is reduced by a factor of 81.67% compared to that of a LCL filter. LLCL filter is becoming attractive for industrial applications due to the possibility to reduce the cost of the copper and the magnetic field material. For a grid-application, the damping losses are less when compared to LCL filter. Since harmonic currents around the switching frequency have been bypassed mostly by the L_f-C_f series-resonant circuit. However, the THD of the grid-current of the LLCL filter based inverter can be lower than that of the LCL filter. The efficiency of the LLCL filter based system is higher than the LCL filter based system due to it's small grid-side inductance.

V. SYSTEM DESCRIPTION

i) PHASE LOCKED LOOP (PLL)

The PLL is used to provide a unity power factor operation which involves synchronization of the inverter output current with the grid voltage and to give a clean sinusoidal current reference. The PLL structure is also used for grid voltage monitoring in order to get the magnitude and the frequency values of the grid voltage.

A phase-locked loop or phase lock loop (PLL) is a control system that tries to generate an output signal whose phase is related to the phase of the input "reference" signal. It is an electronic circuit consisting of a variable frequency oscillator and a phase detector that compares the phase of the signal derived from the oscillator to an input signal. The signal from the phase detector is used to control the oscillator in a feedback loop. The circuit compares the phase of the input signal with the phase of a signal derived from its output oscillator and adjusts the frequency of its oscillator to keep the phases matched.

ii) ADAPTIVE PREDICTOR

The deadbeat controller has similar behaviour to a proportional controller. The introduction of the adaptive predictor as an integral controller to decrease the controlled error of not only the dc but also the ripples brings to the current control implementation a desired robustness against grid voltage distortion and the nonlinearity characteristics of the output voltage of the inverter together with its command.

he adaptive predictor is one kind of FIR (Finite-impulse response) filter. In this current control system, the adaptive predictor is introduced to predict the control error of four sampling peeriods ahead because both the settling time of three sampling periods and and the calculation time delay of one sampling period should be compensated. Moreover, the accuracy of the current control syatem can be improved by subtracting the adaptive predictor output as an adjustment term from the reference current based on the theory of inverse modelling.

In the proposed adaptive predictor, the order is made to be 64, while the data sampling frequency is 64 times source voltage frequency. When increasing the order of the adaptive filter, a higher control accuracy can be made. However, it is also necessary to reduce the order of the filter so that the operation ends in the sampling period. When the order of the adaptive filter is set to 64, the filter window can cover only the grid voltage period. Even if the filter window is decreased to half the grid voltage period, it is still possible to recognize the control error of the second harmonics caused by the unbalance of the grid voltage.

iii) **SPACE VECTOR PULSE WIDTH MODULATION**

The desired three phase voltages at the output of the inverter could be represented by an equivalent vector **V** rotating in the counter clock wise direction as shown in Fig. 3. The magnitude of this vector is related to the magnitude of the output voltage (Fig. 4) and the time this vector takes to complete one revolution is the same as the fundamental time period of the output voltage.

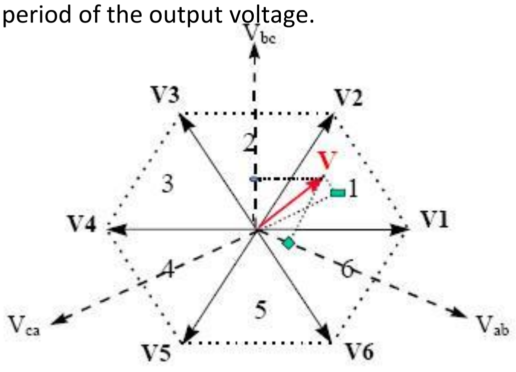


Fig. 3: Output voltage vector in the plane.

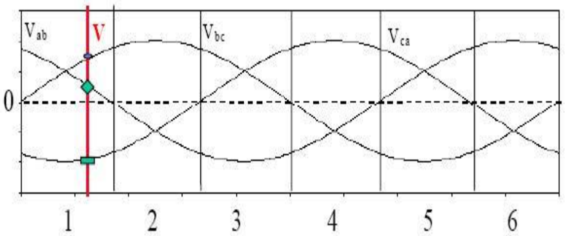


Fig. 4: Output line voltages in time domain.

Let us consider the situation when the desired line-to-line output voltage vector **V** is in sector 1 as shown in Fig. 4. This vector could be synthesized by the pulse-width modulation (PWM) of the two adjacent SSV"s **V1** (pnn) and **V2** (ppn), the duty cycle of each being d1 and d2, respectively, and the zero vector (**V7**(nnn) / **V8**(ppp)) of duty cycle d_0:

$$d_1 v_1 + d_2 v_2 = v = m v_g e^{j\theta} \quad \text{--------(11)}$$

$$d_1 + d_2 + d_0 = 1 \quad \text{--------(12)}$$

Where, *m* = 0.866, is the modulation index. This would correspond to a maximum line-to-line voltage of 1.0Vg, which is 15% more than conventional sinusoidal PWM as shown.

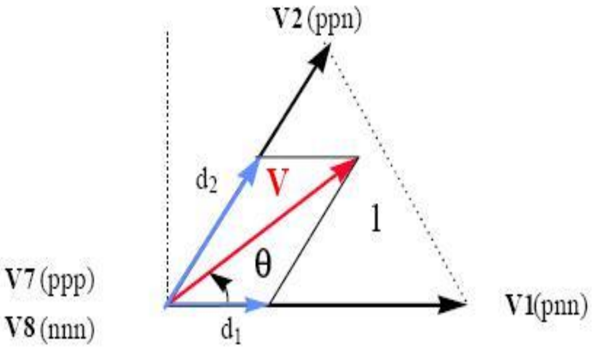


Fig. 5: Synthesis of the required output voltage vector

All SVM schemes and most of the other PWM algorithms use Eqns. (11) and (12) for the output voltage synthesis. The modulation algorithms that use non-adjacent SSV"s have been shown to produce higher THD and/or switching losses and are not analyzed here, although some of them, e.g. hysteresis, can be very simple to implement and can provide faster transient response. The duty cycles d1, d2, and d0, are uniquely determined from Fig. 5, and Eqns. (11) and (12) , the only difference between PWM schemes that use adjacent vectors is the choice of the zero vector(s) and the sequence in which the vectors are applied within the switching cycle.

VI. CIRCUIT PARAMETERS

L_1 = 5mH	D.C link voltage =220V
L_2 = 3mH	Grid voltage = 200v rms
L_f = 5mH	Grid frequency = 50HZ
C_f = 12µF	Switching frequency = 3.84 KHZ

VII. SIMULATION RESULTS:

i. Inverter Mode of Operation:

Fig. 6 demonstrates a run-back power system. As the 12-pulse rectifier is used as the former converter in the run-back system, the output current reference of the inverter as the latter converter can be set arbitrarily, and the performance of the utility inverter with the new control scheme treated here can be easily and accurately tested. The utility interactive inverter employs the synchronous space vector pulsewidth modulation (PWM). When using the PLL circuit, one grid voltage period is divided into 128 PWM periods, and one PWM period is divided into 256 steps equally. The data sampling timing is synchronous with PWM, and the sampling frequency is $64 \times f = 3840$ Hz.

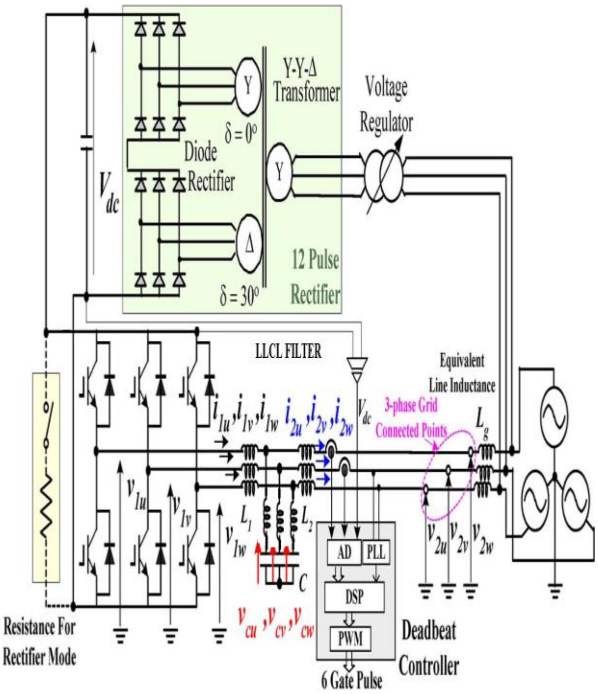


Fig.6: Run-back power system for grid-connected inverter through LLCL filter.

i) INVERTER MODE OF OPERATION:

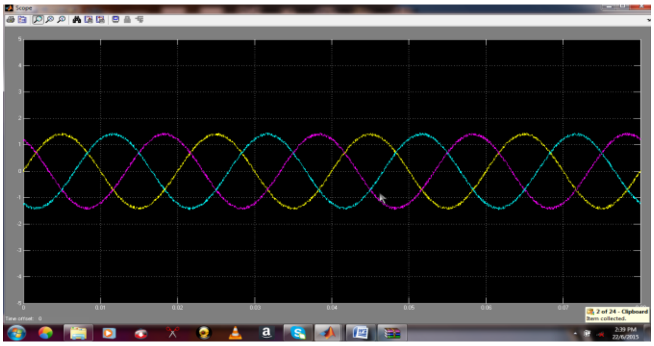


Fig.a) open loop mode (i_2THD=1.13%)

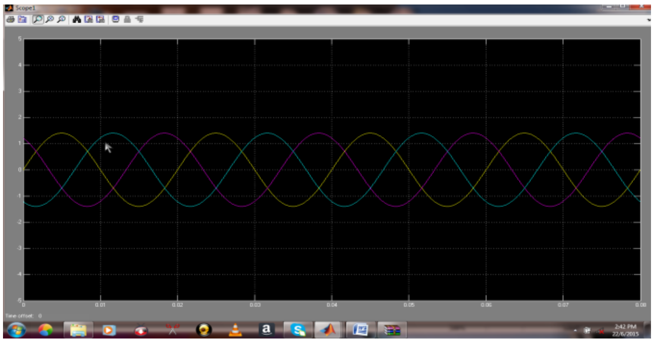


Fig.b) Introduction of Deadbeat system without adaptive predictor (i_2THD=1.10%)

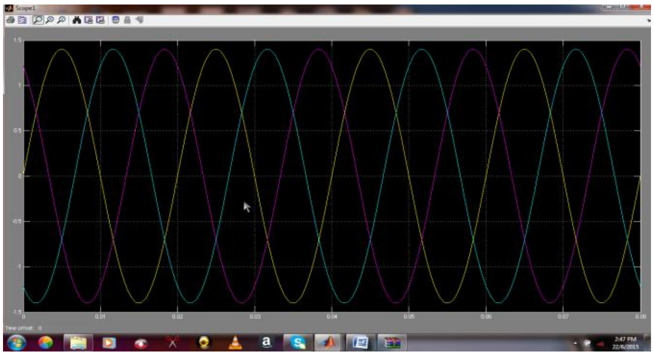


Fig.c) Deadbeat system with adaptive predictor (i_2THD=0.73%)

ii) STATCOM MODE OF OPERATION:

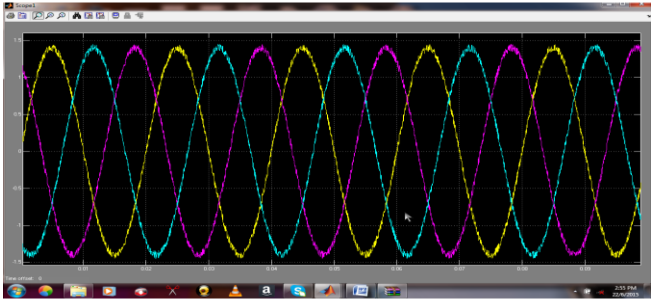


Fig.a) open loop mode (i_2THD=2.94%)

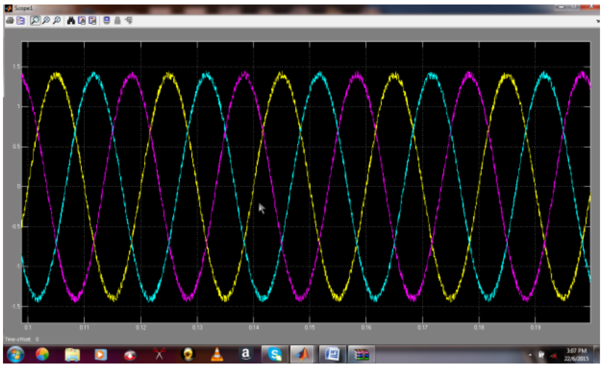


Fig.b) Introduction of Deadbeat system without adaptive predictor (i_2THD=1.88%)

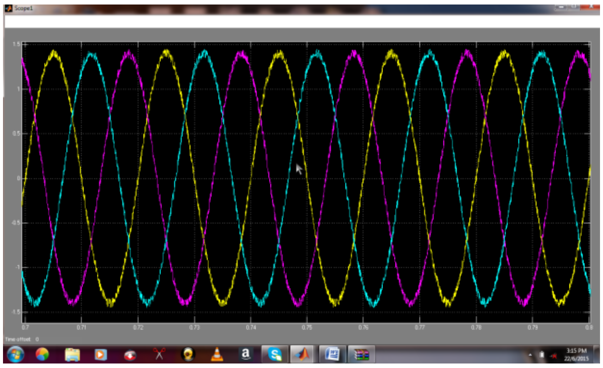


Fig.c) Deadbeat system with adaptive predictor (i_2THD=1.44%)

iii) RECTIFIER MODE OF OPERATION:

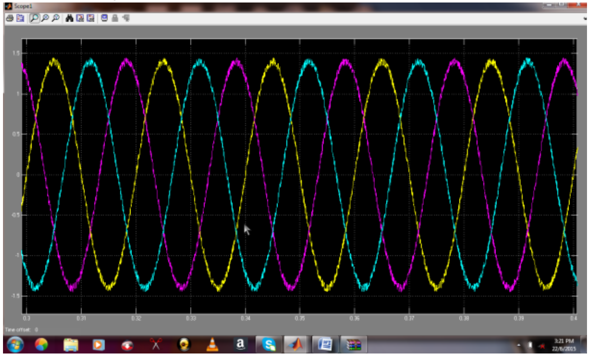


Fig.a) Before step change (i_2THD=1.93%)

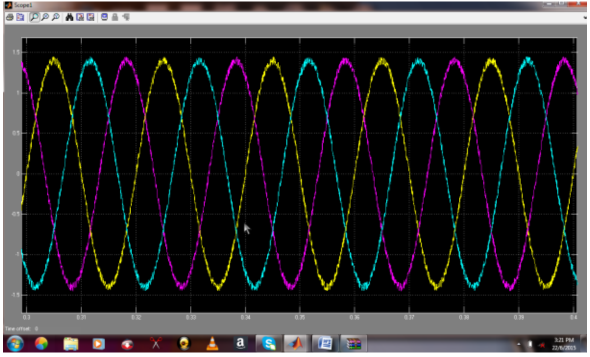
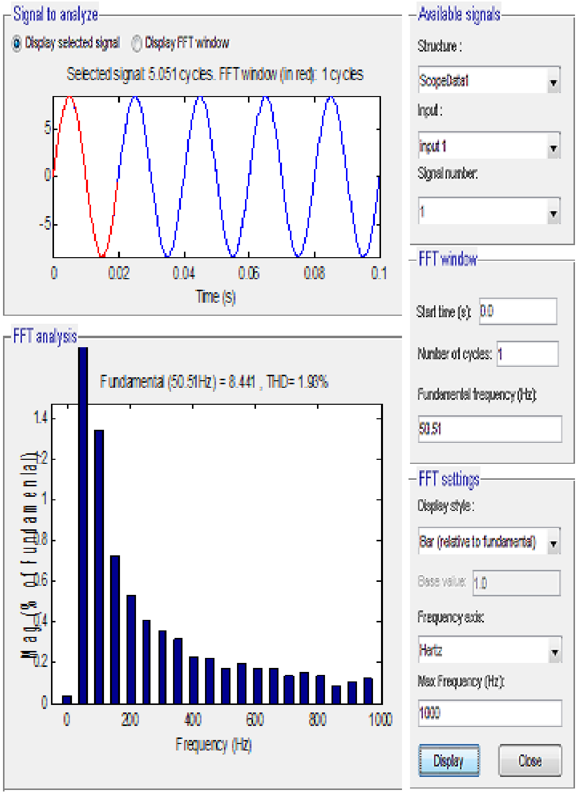


Fig.c) After step change (i_2THD=0.8%)



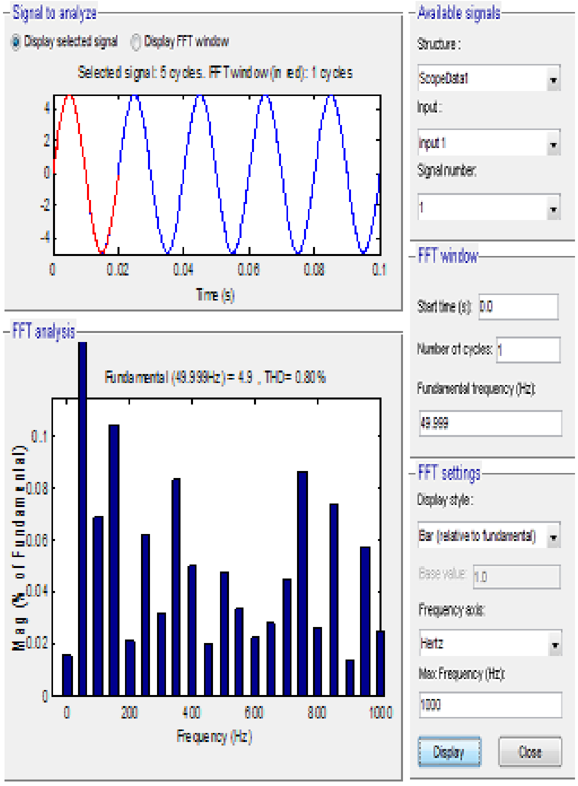
Signal to analyze
● Display selected signal ○ Display FFT window
Selected signal: 5.051 cycles. FFT window (in red): 1 cycles

FFT analysis
Fundamental (50.51Hz) = 8.441 , THD= 1.93%

Available signals
Structure: ScopeData1
Input: input 1
Signal number: 1

FFT window
Start time (s): 0.0
Number of cycles: 1
Fundamental frequency (Hz): 50.51

FFT settings
Display style: Bar (relative to fundamental)
Base value: 1.0
Frequency axis: Hertz
Max Frequency (Hz): 1000



Signal to analyze
● Display selected signal ○ Display FFT window
Selected signal: 5 cycles. FFT window (in red): 1 cycles

FFT analysis
Fundamental (49.999Hz) = 4.9 , THD= 0.80 %

Available signals
Structure: ScopeData1
Input: input 1
Signal number: 1

FFT window
Start time (s): 0.0
Number of cycles: 1
Fundamental frequency (Hz): 49.999

FFT settings
Display style: Bar (relative to fundamental)
Base value: 1.0
Frequency axis: Hertz
Max Frequency (Hz): 1000

Fig.d) FFT analysis for rectifier mode after step change

VIII. COMPARISON OF THD OBSERVED ON GRID CURRENT FOR LLCL AND LCL FILTERS

MODE OF OPERATION	THD LEVEL	
	LLCL FILTER	LCL FILTER
INVERTER	0.73%	1.5%
STATCOM	1.44%	2.1%
RECTIFIER	0.8%	1.2%

IX.CONCLUSION

In this paper, the principle of the conventional LLCL filter is presented. It can be seen that the main high-order harmonic currents mostly appear around the switching frequency. Based on this, a new topology of low-pass power filter with Lf –Cf series resonant circuit, named the LLCL filter, has been proposed. In contrast to the LCL filter, the LLCL filter has nearly zero impedance at the switching frequency and can strongly attenuate the harmonic currents around the switching frequency when compared to the conventional LCL filter.

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