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REVIEW ARTICLE

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A NOVEL APPROACH FOR SYMMETRICAL VIRTUAL RAIL CLAMPING AND 'LECTOR' BASED TECHNIQUE WITH H-SPICE TOOL

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ABSTRACT

The approach describes the leakage power reduction using a technique called LECTOR. In this method two leakage control transistors are used. The pMOS transistor is placed at the header and the nMOS transistor is at the footer. This paper compares the symmetrical virtual rail clamping technique and the LECTOR technique where the latter does not need any additional control and limits the area increase, power dissipation when it is in active state. The leakage power is reduced by 54% and the simulation is done using H-spice tool.

Key Words—Active mode, leakage power, power gating, , threshold voltage, virtual rail clamping, LCT

I. INTRODUCTION

Power gating technique has been a popular method for reducing the leakage power when the system is in active mode (when it is doing a useful work). It is examined with a CMOS(Complementary Metal Oxide Semiconductor). The dynamic power is the power consumed by switching gates and the leakage power is the power consumed by the gates which is in sleep mode [1]. The power is obtained by adding the sleep transistors between the circuit and the headers/footers. It gives the average leakage power without any necessity for an alteration to the logic or operation of the power gated circuit. Here the performance is seriously impacted and applied only for the non-performance constrained application. In this paper, a technique called sub-clock power gating (SCPG) is used where the application mainly focuses on low power consumption. Anyhow the performance is not so critical. The main application is wireless sensor nodes and bio-medical sensor nodes in which the main goal is power consumption.

The power gating methods are i) Fine grain power gating ii) Coarse grain power gating.. In a coarse-grained power gating, a software-dependent sleep modes are made which will turn off the system during the large idle periods [2]. But it has some issues in timing when power gating the cluster of cells which is difficult to solve. These cells design becomes the standard cell rules done by EDA tools. The low voltage devices have to be used if there are multiple voltage libraries. The coarse grained approach involves the grid style sleep transistors. It is less sensitive to PVT (Performance Verification

Test) variation and produces less IR-drop, area overhead than the cluster based approaches. It has two ways of implementation: Ring-based, Column-based. Gate sizing rely on switching current of a design.

To reduce the simultaneous switching, gate control buffers should be daisy chained. Section II, describes the of symmetrical virtual rail clamping . Section III, describes the LECTOR based approach and the leakage power calculation.

II.Symmetrical virtual rail clamping

The symmetrical virtual rail clamping employs the pair of transistors at the head and the foot of the inverter. Always the virtual rail clamping gives a single threshold voltage drop reduction to reduce the clamped voltage. The power gated circuit is connected to the supply rail through high V_t pMOS sleep transistor. It disables the high V_t transistor during extended idle periods reducing the leakage power further given in Fig.1. When Sleep=Ret=logic 1(nSleep=nRet=0), the VV_{dd} is clamped to V_{dd}-V_{thn} and VV_{ss} is clamped to V_{ss}+V_{thp}.

The advantages over single virtual rail clamping is the supply rail is recycled to charge up VV_{ss} in sleep mode [6].Thus the average leakage power obtained is given by 3.4559E-05W.. However , the proposed symmetrical virtual rail clamping has a greater leakage power saving which is attributed to the exploitation of reverse body biasing of both nMOS and pMOS transistors which is described in Fig. 2.

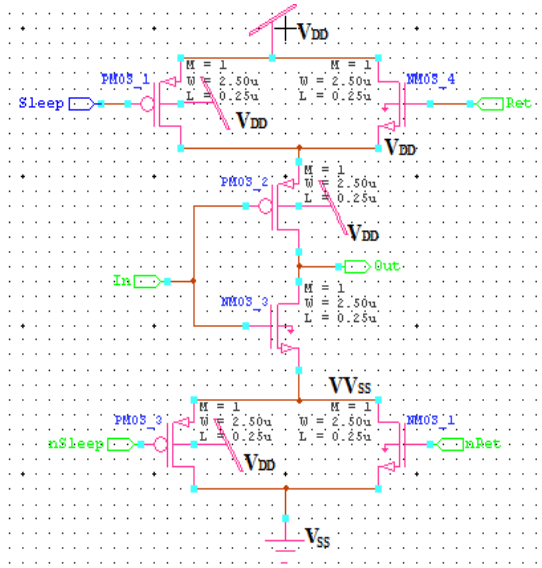

Fig 1. Symmetrical virtual rail clamping

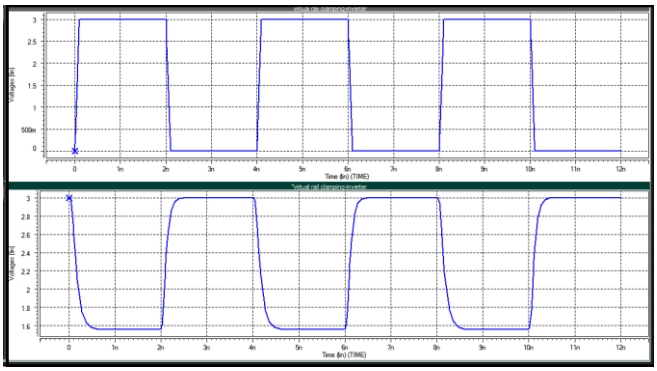

Fig. 2. Output of symmetrical virtual rail clamping

III. LECTOR based approach

The effective stacking of transistors in the path from supply voltage to ground is the basic idea behind the LECTOR technique for the leakage power reduction. In this technique, two leakage control transistors are introduced between pull-up and pull-down network within the logic gate (one PMOS for pull-up and one NMOS for pull-down) for which the gate terminal of each leakage control transistor (LCT) is controlled by the source of the other. This arrangement ensures that one of the LCTs always operates in its near cutoff region. Two LCTs are introduced between nodes N1 and N2. The gate terminal of each LCT is controlled by the source of the other, hence termed as self-controlled stacked transistors. As LCTs are self-controlled, no external circuit is needed; thereby the limitation with the sleep transistor technique has been overcome.

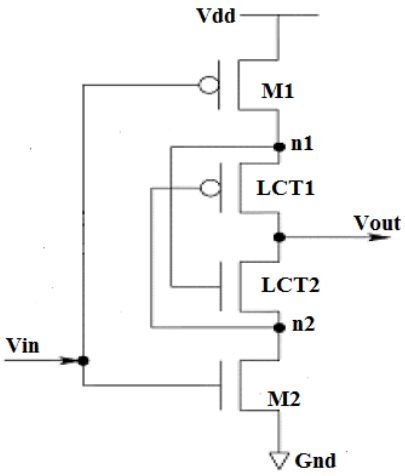

Fig .3. A lector inverter

The introduction of LCTs increases the resistance of the path from Vdd to Gnd, thus reducing the leakage current. Leakage Control Transistor (LECTOR) technique is illustrated in detail with the case of an inverter. A LECTOR INVERTER is shown in Fig.3. A PMOS is introduced as LCT1 and a NMOS as LCT2

between N1 and N2 nodes of inverter. The output of inverter is taken from the connected drain nodes LCT1 and LCT2. The source nodes of LCT1 and LCT2 are the nodes N1 and N2 respectively of the pull-up and the pull-down logic. The gates of LCT1 and LCT2 are controlled by the potential at source terminal of LCT2 and LCT1 respectively [10]. This connection always keeps one of the two LCTs in its near cutoff region for any input.The leakage power calculated is 2.2039E-05W. The simulation tool is H-spice is a set of analysis and design capabilities that support the design of high-speed circuits.

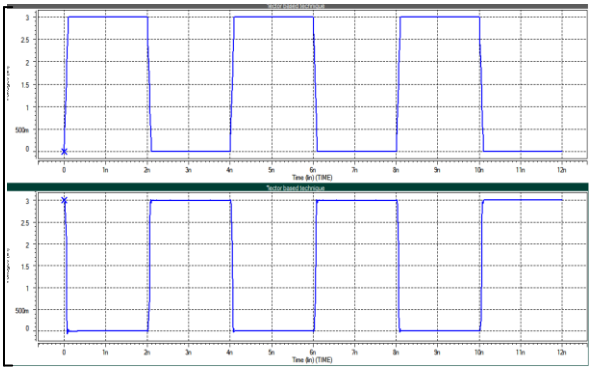

Fig. 4 .Output of Lector based approach

AvanWaves analyzes and display the waveform of the proposed system and print the H-spice simulation output [8]. Dynamic power is essential during normal mode, particularly at high frequencies, but static power is needed during sleep mode, mainly for battery related circuits [9].

IV. CONCLUSION

The project has been successfully simulated and the average power has been compared for symmetrical virtual rail clamping and the lector based approach and noted that 54% of the leakage power has been reduced. LECTOR achieves the reduction in leakage power like other leakage reduction techniques, such as sleepy stack, sleepy keeper, etc, along with the advantage of not affecting the dynamic power, since this technique does not require any additional control and monitor circuitry and also in this technique, the exact logic state is maintained.

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