International Journal of Engineering Research-Online
A Peer Reviewed International Journal
Articles available online http://www.ijoer.in

Vol.3., Issue.2, 2015

RESEARCH ARTICLE

ISSN: 2321-7758

IMPLEMENTING EFFICIENT EMBEDDED LOGIC IN LOW POWER TWIN DYNAMIC PULSED HYBRID FLIP-FLOP

SATHIA PRIYA .M[1], SRIDEVI.A[2], BINI JOY[3]

[1,2,3]DEPARTMENT OF ECE, M.E (VLSI Design), SNS College of Technology, Coimbatore, Tamil Nadu, India.

Article Received: 12/04/2015 | Article Revised on:17/04/2015 | Article Accepted on:20/04/2015

ABSTRACT

Flip Flops are critical timing elements in digital circuits which have large impact on circuit speed and power consumption. The parameters to be considered while designing a flip flop is power and delay. The proposed Twin Dynamic pulsed hybrid Flip Flop(TDFF) eliminates the large capacitance present in the precharge node due to its split dynamic node structure. It eliminates the redundant power dissipation present in Cross Charge control flip flop(XCFF). TDFF provides short latency and logic functions can be incorporated with minimum delay. A novel embedded logic module(TDFF-ELM) based on TDFF is implemented which is used to reduce pipeline overhead. The performance of the flip flops are analysed using TANNER EDA tools.

Keywords : Flip Flop,Embedded logic module,power,delay

1.INTRODUCTION

Latches and flip-flops are the basic elements for storing information. One latch or flip-flop can store one bit of information. The main difference between latches and flip-flops is that for latches, their outputs are constantly affected by their inputs as long as the enable signal is asserted. In other words, when they are enabled, their content changes immediately when their inputs change. Flip-flops, on the other hand, have their content change only either at the rising or falling edge of the enable signal. This enable signal is usually the controlling clock signal. After the rising or falling edge of the clock, the flip-flop content remains constant even if the input changes. There are basically four main types of latches and flip-flops: SR, D, JK, and T. The major differences in these flip-flop types are the number of inputs they have and how they change state.

1.1 Requirements Of Flip Flop Design

Flip-flops (FFs) are the basic storage elements used extensively in all kinds of digital designs. In particular, digital designs nowadays often adopt intensive pipelining techniques and employ many FF-rich modules such as register file, shift register, and first in first out. It is also estimated that the

power consumption of the clock system, which consists of clock distribution networks and storage elements, is as high as 50% of the total system power. FFs thus contribute a significant portion of the chip area and power consumption to the overall system design.The requirements of designing a flip flop are as follows.

- Minimum flip flop overhead ,small clk-q delay,small setup time,small hold time
- Minimum power
- High driving capability
- Cross talk sensitivity
- Small load on clock to improve the performance of clock and reduce the power of clock

2.EXISTING METHODS

2.1 POWER PC 602 FLIPFLOP

In order to overcome the problem of distributing several clock signals and avoid the problems caused by clock skew, a NORA-CMOS introduced a technique called True Single Phase Clock (TSPC) CMOS circuit technique TSPC flip-flops have the advantage of single clock distribution, , high speed and no clock skew. It show implementation of eight-transistor positive edge-triggered D flip-flop using split-output TSPC latches.

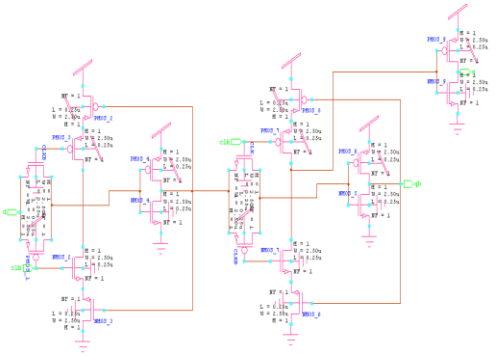

Fig. 1 Schematic of Power PC 602 Flip Flop

This structure occupies smaller area and lower number of clocked transistors . The drawback is that some nodes in are not fully driven to VDD or GND.The Fig. 1 is the circuit diagram of Power PC 602 FlipFlop. This is known as static flip flops.

2.2 SEMI DYNAMIC FLIPFLOP(SDFF)

The circuit shown in the Fig. 2 consists of a dynamic frontend and a static backend. It samples input signal D and produces output signal QB, which is the complement of D. During the falling edge of clock CLK, the flip flop enters the precharge phase. At that time X is precharged high, disabling Q from the input stage. The static latch inverter holds the previous logic level of Q and QB. Since CKD is also low during precharge phase, node S remains high holding keeping transistor N1 on. If input D is low then node X remain high.Node Q would either remain low or will be discharged through transistors N4 and N5, driving QB high.

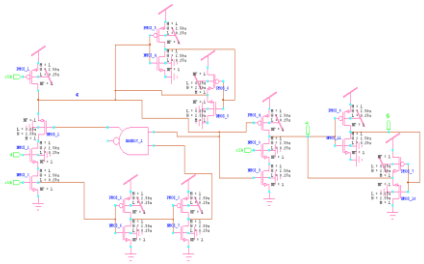

Fig. 2 Schematic of Semi Dynamic Flip Flops(SDFF)

3.PROPOSED METHOD

3.1 TWIN DYNAMIC PULSED HYBRID FLIP FLOP(TDFF)

The circuit diagram of Twin Dynamic Hybrid Flip Flop (TDFF) is shown in Fig. 3. QB in the output is inverted by INV2, has the output as Q. So the output Q is again inverted and causes error when it's connected to QB.

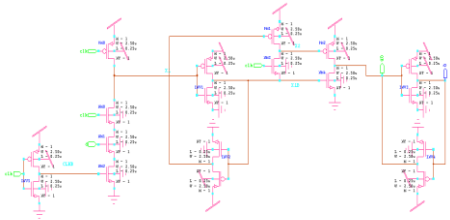

Fig. 3 Schematic of Twin Dynamic Pulsed Hybrid Flip Flop(TDFF)

In TDFF architecture the node X1 is pseudo-dynamic structure, having a weak inverter as a keeper, whereas, compared with other flipflop architecture which have node X2 as purely dynamic. A shutoff mechanism is provided at the frontend whereas conditional one in XCFF. The operation of the flip-flop is being divided into two phases.The first phase is evaluation phase, during which CLK is high, and the second is precharge phase, during which CLK is

low. The actual latching occurs during the overlap of CLK and CLKB at the time of evaluation phase. Node X1 is discharged through NM0 which switches the state of the inverter pair INV1 and INV2 causing node X1 to go high and output QB to discharge through NM4. The lower level at the node X1 is retained by the inverter pair INV1and INV2 and no latching occurs during the other phase of evaluation and so, node X2 is held high throughout the evaluation period by the PMOS transistor. While CLK goes low, the circuit is in precharge phase and node X1 is pulled high through PM0, switching the state of INV1 and INV2.

During this period node X2 is not driven by any transistor and dynamically it stores the charge. The outputs at node QB maintain their voltage levels through inverter pairs. If D is zero then, node X1 remains high and node X2 is pulled low through NM2 when CLK goes high. Thus, node QB is goes high through PM2. At the end of the evaluation phase, as the CLK falls low, node X1 remains high and X2 stores the charge dynamically. The structure exhibits negative setup time since the short transparency period defined by the overlap of CLK and CLKB allows the data to be sampled even after the rising edge of the CLK before CLKB falls low.

3.2 TWIN DYNAMIC PULSED HYBRID FLIP FLOP WITH EMBEDDED LOGIC MODULE(TDFF-ELM)

Many functions have been embedded into the proposed flip flop architecture to analyze the performance of the structure in terms of power and speed. SDFF has a fast non inverting output and a slow inverting output, whereas the proposed flip flop architecture has a fast inverting output and a slow non inverting output. The comparison of delay of, inverting and non inverting outputs were considered for SDFF and the proposed architecture. AND, OR functions and a two-input multiplexer were embedded into both the designs by replacing the respective PDN structures shown in Fig. 4 . It is used to reduce pipeline overhead .

Since TDFF-ELM performs the function of a flip-flop when no logic is embedded into it.The performance as a flip-flop is compared with other flip-flops along with TDFF. TDFF-ELM was designed using three inverters for generating sampling window. In order to depict the advantages of embedding logic in to the flip-flop, the combinations of static logic and flip-flop, performing the same functions, are also designed. The performance of this discrete combination is also analysed and compared with the embedded functions.

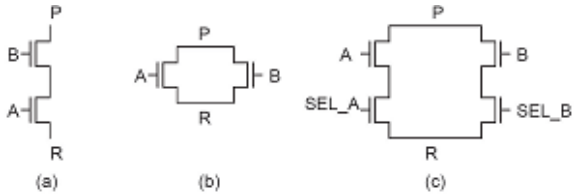

Fig. 4 Embedded Functions (a)AND (b)OR (c)2:1 Multiplxer

The structure of the proposed Twin dynamic node hybrid flip-flop with logic embedding capability (DDFF-ELM) is shown in Fig. 5. Note that in the new model, the transistor driven by the data input is replaced by the PDN and the clocking scheme in the frontend is changed. The reason for this in clocking is the charge sharing, which becomes uncontrollable as the number of NMOS transistors in the stack increases. The same reason makes XCFF also incapable of embedding complex logic functions. In order to get a clear picture of the charge sharing in XCFF , it was simulated with different embedded functions.

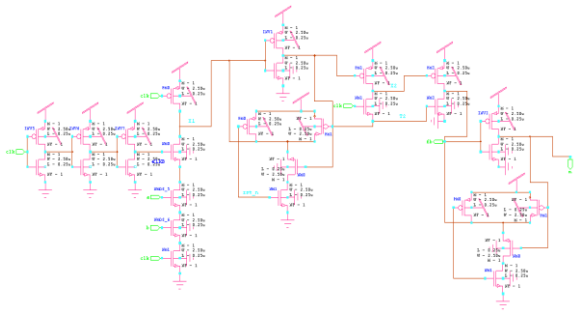

Fig. 6 Schematic of Twin Dynamic Pulsed Hybrid Flip Flop with embedded logic module(TDFF-ELM)

4. SIMULATION RESULTS

4.1 TWIN DYNAMIC PULSED HYBRID FLIP FLOP

TDFF is the proposed flip flop structure and the waveform is shown in the Fig. 7.The inputs given to

the circuit are CLK and D and their respective outputs are Q and QB.

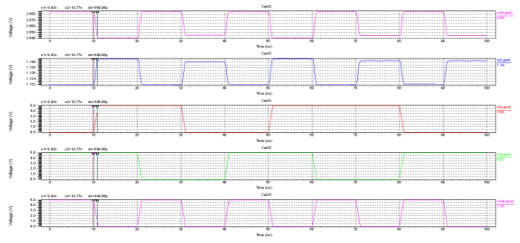

Fig. 7 Output waveform of TDFF

4.2 TWIN DYNAMIC PULSED HYBRID FLIP FLOP WITH ELM

Embedded logic module in implemented in TDFF and the inputs given are CLK and D and their corresponding outputs are Q and QB shown in the Fig. 8.

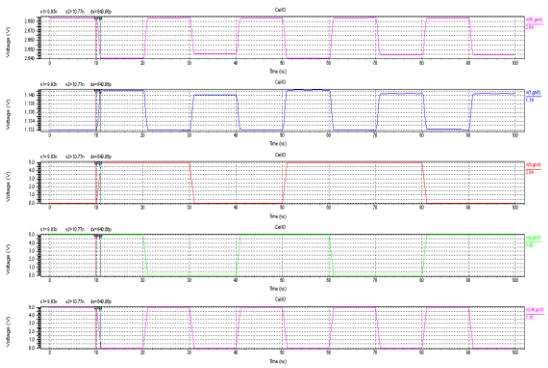

Fig. 8 Output waveform of TDFF-ELM

From the simulation results it is clearly understood that Twin Dynamic pulsed hybrid flip flop(TDFF) module has minimum power consumption and delay so it is shows better efficiency when embedded logic module is implemented in it.

4.3 COMPARISON TABLE

TABLE I: COMPARISON OF FLIP FLOPS

Flip Flops	Number Of Transistors	Total Power (mW)	Minimum D-Q (s)
POWERPC 603	20	15.9	1.18(p)
SDFF	19	5.44	1.18(p)
TDFF	22	6.48	840.3(n)
TDFF-ELM	**23**	**1.10**	**840.5(n)**

5. CONCLUSION AND FUTURE ENHANCEMENT

5.1 CONCLUSION

A new low power TDFF and a novel TDFF-ELM are proposed and comparison of the proposed flip-flop with the conventional flip-flops showed that it exhibits lower power dissipation along with comparable speed performances. By eliminating the charge sharing, the revised structure of the proposed flip-flop, TDFF-ELM, is capable of efficiently incorporating complex logic in to the flip-flop with minimum delay.The power delay product is greatly reduced in the proposed method while comparing with all other flip flop structures.

5.2 FUTURE ENHANCEMENT

The efficiency of the flip-flop and the ELM will show better efficiency by using it in the design of 4-b synchronous counter and a 4-b Johnson up-down counter. It shows that the proposed architectures are well suited for modern high performance designs where area, delay-overhead, and power dissipation are of major concern.

REFERENCES

[1] Kalarikkal Absel, Lijo Manuel,"Low Power Dual Dynamic Node Pulsed Flip-Flop featuring efficient embedded logic". 2013; 21(9).

[2] G. Gerosa, S. Gary, C. Dietz, P. Dac, K. Hoover, J. Alvarez, H. Sanchez, P. Ippolito, N. Tai, S. Litch, J. Eno, J. Golab, N. Vanderschaaf, and J. Kahle, "A 2.2 W, 80 MHz superscalar RISC microprocessor," IEEE J. Solid-State Circuits, vol. 29, no. 12, pp. 1440–1452, Dec. 1994.

[3] M. Hansson and A. Alvandpour, "Comparative analysis of process variation impact on flip-flop power-performance," in Proc. IEEE Int. Symp. Circuits Syst., May 2007, pp. 3744–3747.

[4] F. Klass, "Semi-dynamic and dynamic flip-flops with embedded logic," in Proc. Symp. VLSI Circuits Dig. Tech. Papers, Honolulu, HI, Jun. 1998, pp. 108–109.

[5] B.-S. Kong, S.-S. Kim, and Y.-H. Jun, "Conditional-capture flip-flop for statistical

power reduction," IEEE J. Solid-State Circuits, vol. 36, no. 8,pp. 1263–1271, Aug. 2001.

[6] H. Mahmoodi, V. Tirumalashetty, M. Cooke, and K. Roy, "Ultra lowpower clocking scheme using energy recovery and clock gating," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 17, no. 1, pp. 33–44, Jan. 2009.

[7] A. Ma and K. Asanovic, "A double-pulsed set-conditional-reset flipflop," Laboratory for Computer Science, Massachusetts Inst. Technology, Cambridge, Tech. Rep. MIT-LCS-TR-844, May 2002.

[8] H. Patrovi, R. Burd, U. Salim, F. Weber, L. DiGregorio, and D. Draper, "Flow-through latch and edge-triggered flip-flop hybrid elements," in Proc. IEEE ISSCC Dig. Tech. Papers, Feb. 1996, pp. 138–139.

[9] V. Stojanovic and V. Oklobdzija, "Comparative analysis of masterslave latches and flip-flops for high-performance and low-power systems,"IEEE J. Solid-State Circuits, vol. 34, no. 4, pp. 536–548, Apr. 1999.

[10] J. Yuan and C. Svensson, "New single-clock CMOS latches and flipflops with improved speed and power savings," IEEE J. Solid-State Circuits,vol. 32, no. 1, pp. 62–69, Jan. 1997.