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RESEARCH ARTICLE

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EXECUTION OF BIST TECHNIQUE AND AUTOMATIC RECOGNITION OF BAUD RATE IN UART

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ABSTRACT

In the field of electronic configuration, SOC innovation is as of late getting to be progressively full grown. This circumstance brings about the prerequisite of understanding the entire framework work in a solitary or a not very many chips. Universal asynchronous Receiver Transmitter (UART) is a sort of serial correspondence convention. In any case because of the blunders delivered in the yield of the information got the circuits are as a rule not performed well in the capacities to diminish the likelihood of item disappointments and missed business sector opportunities by giving the need to guarantee the information to be moved in blunder confirmation. So with the proposed structural planning of BIST in UART we can decrease extravagant analyzer prerequisites and testing techniques in circuit are minimized and it takes out the need to gain top of the line analyzers. This paper focuses on building up a serial correspondence convention (UART) with programmed baud rate discovery. Programmed baud rate identification is valuable for securing correspondence connect between two devices. The slave's gadget will ready to recognize the baud rate of the expert controller and modify accordingly. UART widespread offbeat beneficiary transmitter is for the most part utilized for better transmission of serial information that is either transmit or get information serially. It includes outlining of essential modules utilizing Very High Speed Integrated Circuit Hardware Description Language (VHDL).

Keywords— SOC, FPGA, UART, VHDL

I. INTRODUCTION

Serial communication reduces the distortion of a signal, therefore makes data transfer between two systems separated in great distance possible. A universal asynchronous receive/transmit (UART) is an integrated circuit which plays the most important role in serial communication. It handles the conversion between serial and parallel data.

At the point when the transmitter is sit still, the information line is in high rationale state. If not when an expression is given to the UART for non concurrent transmissions, "begin bit" is added to the

start of every statement that is to be transmitted. The begin bit is utilized to known the peripherals recipient that an expression of information is going to be sent, and synchronization is to constrain the check in the beneficiary to synchronize with the check in the transmitter. After the begin bit, the information bits of the saying are sent, with the minimum critical bit (LSB) being sent first. Every bit is transmitted at precisely same time as the greater part of alternate bits, and the beneficiary specimens at the wire at half of the way finished with the period doled out to every bit to figure out whether the bit is a 1 or a 0.when the whole information word has been sent, the transmitter includes an equality bit that the transmitter produces. The equality bit may be utilized by the beneficiary to perform straightforward lapse checking then one stop bit is sent by the transmitter.

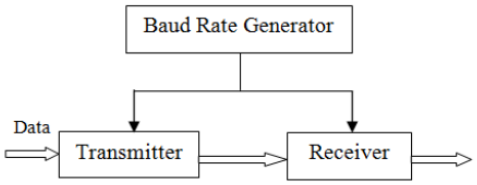

Fig1: UART Module

When the receiver has received all of the bits in the frame, it automatically discards the start, parity and stop bits. If another word is ready for transmission, the start bit for the next word will be sent when the stop bit for the before transmitted bits or data is received**.** In actual applications, usually a few features in UART are required. Specific interface chip causes increase in cost and wastage of resources in electronic design, SOC technology is being used widely now-a days. This shows the requirement of realizing the whole system function in a single or a few chips. Manufacturing process is extremely complex, for the manufacturers even to consider testability requirement to have the reliability and the functionality of each of their designed circuits.

In the new system-on-a-chip design, many cores are integrated into a single chip. As ICs grow in gate counts, it is no longer true that most gate nodes are directly accessible by one of the pins on the package. This makes testing of the nodes more difficult as they could be no longer be easily observed by signal from an input pin nor easily observed at an output pin. UART is a fringe gadget serial port with settled baud rate. It is an incorporated circuit utilized for serial correspondence more than a PC or fringe gadgets. It comprises of a transmitter, collector, also every timed independently. It transmit 9600 to 38400 bps for transmitting information bit. UART changes over the bytes of information into a single serial bit. It includes an equality bit amid the transmission and check the equality bit and dispose of it, furthermore it includes begin bit amid the transmission , keeping in mind the end goal to ready that recipient that an expression of information is going to be send furthermore it handles hinder furthermore gadget administration.

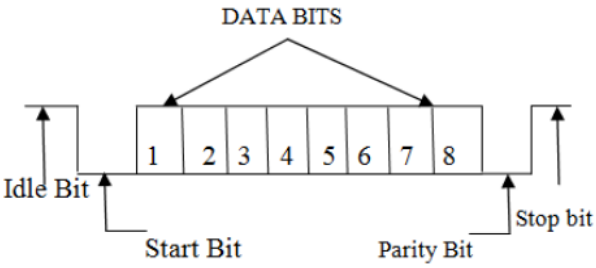

Fig2: UART Frame Formate

That co-organizing the PCs paces of operation with gadget speeds. There are two methods for transmitting a byte between two advanced gadgets. That is serial and parallel correspondence. Parallel correspondence motivations sending an entire byte of information over various wires and every bit has a solitary wire given to it and all bits are transmitted in the meantime. Then again serial correspondence is that help us to send information to remote gadget by sending information bit more than a solitary wire. at the point when UART is working with altered baud rate for the transmitter ,as the baud rate of the transmitter changes the recipient can't conform with the expert naturally the time it now, lengthy furthermore there is a chance for information misfortune. So we strive for the outline of FIFO based UART With programmed baud rate identification. Programmed location is helpful for securing correspondence interface between two gadgets .The slave gadget will have the capacity to identify the baud rate of the expert controller and change as needs be.

II. BIST TECHNIQUE

In VLSI we have testing problems like input combinatorial problems, gate to I/O pin ratio problems, Test generation problems, led the designer to identify reliable test methods and solve this problems.teh insertion of special test circuitry

on the VLSI circuits that allows efficient test methods. This has been addressed by the need for design for testability (DFT) and hence the need for BIST. It tests the circuit or system function itself hence it is named as “self-test".BIST is an on-chip test logic that is utilized to test the functional logic of a chip, by itself. Due to the rapid increase in the design complexity, BIST has become a major design consideration in DFT methods and is becoming increasingly important in today’s state of the art SoCs. A properly designed BIST is able to offset the cost of added test hardware while at the same time ensuring the reliability, reduces maintenance cost and testability.

UART Architecture With BIST:

The architecture proposes an 8-bit UART which operates at a baud rate of 9600 bps with a status register to monitor the correctness of every received data byte and enhance the testability of circuit by the introduction of BIST module. The proposed model has two major modules like UART and BIST. Further in the UART, we have transmitter, Receiver, and baud rate generator as discussed before. Baud rate generator works at 50 MHz and further reduced as required for the operations in transmitter and receiver to achieve baud rate of 9600 bps. BIST has a control register, pattern generator and a comparator.

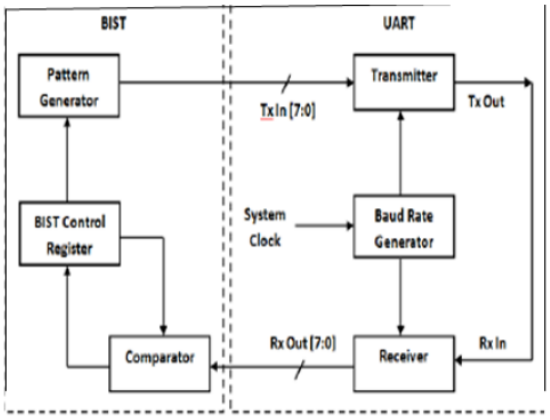

Fig3: UART with BIST technique

BIST Pattern Generator:

In BIST session where the example generator is one of the module in it which it delivers pseudo–random test designs by utilizing LFSR as the test design generator. A LFSR is a movement generator where its include is a straight capacity of two or more bits which are called as taps. It comprises of the D-flip-flop and the ex-or doors in its capacity. It performs its operation by moving the bits and ex-or operation, In LFSR we have two sorts they are inner LFSR and outside LFSR. Here we are utilizing outer LFSR the bits contained in chose positions in the outcome is nourished go into the register's data bit. The bit positions chose for utilization in the input capacity are called "taps". The biggest state space feasible for such a LFSR will be 2^n-1, all conceivable qualities aside from zero state are indicated as an illustration. A grouping of paired numbers can be spoken to utilizing an era function(polynomials).The conduct of a LFSR is controlled by its introductory "seed" and its input coefficients, both can be spoken to by polynomials. Every one of the zero qualities is not permitted in LFSR, as it generally deliver 0 in spite of what number of clock cycle. Since every state can have stand out succeeding express, a LFSR with a maximal length tap grouping will go through every non-zero state once and just once before again rehashing an alternate state. In LFSR the test arbitrary test design generators are produced by the ex-or and D-flip lemon operation and the created examples are sent as information to the transmitter segment in the UART module.

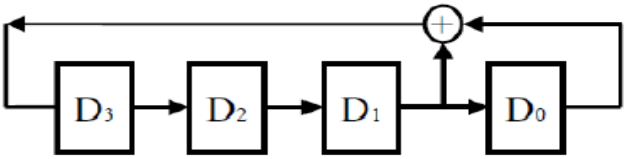

Fig4: LFSR example

UART Transmitter:

The transmitter accepts parallel data from the test pattern generator which generates pseudo random test patterns as input, and then it makes the frame of the data and transmits the data in serial form on the Transmitter Output (TXOUT) terminal shown in Fig.5. The baud rate generator output will be the clock for UART transmitter.

Data is loaded from the parallel inputs TXIN0-TXIN7 into the Transmitter FIFO by applying logic high(1) on the WR (Write) input. FIFO is 16-byte register. If FIFO is full, it sends FIFO Full (FF) signal to peripheral as shown in Fig. 5. When FIFO contains some data, it will send the signal to Transmitter Hold Register (THR), which is an 8-bit register. At the same time, if THR is empty it will send the signal to FIFO, back which indicates that THR is ready to receive data from FIFO. If Transmitter Shift Register (TSR) is empty, it will send the signal to THR and it indicates

that TSR is ready to receive data from THR. TSR is an 11-bit register in which framing process occurs. In frame, start bit, parity bit and one stop bit will be added . Now data is transmitted from TSR to TXOUT serially. From the transmitter the data is sent to the UART receiver as the loopback function where the baud rate acts as a clock for the synchronization between the transmitter and the receiver to receive data correctly.

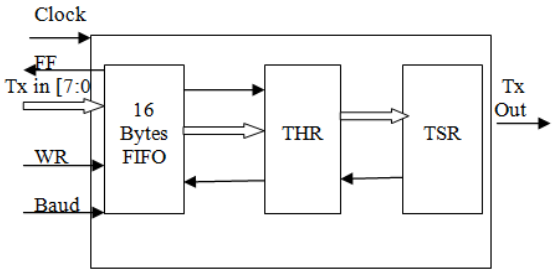

Fig5: UART Transmitter

UART Receiver:

The received serial data is available on the RXIN pin. The received data is applied to the sampling logic block. The receiver timing and control is used for synchronization of clock signal between transmitter and receiver. The receiver sampling is 16 times to that of the transmitter baud rate. In the architecture of UART receiver Fig.6 initially the logic line (RxIn) is high. Whenever it goes low sampling and logic block will take 4 samples of that bit and if all four are same it indicates the start of a frame. After that remaining bits are sampled in the same way and if all the bits are sent to Receiver Shift Register (RSR) one by one where the entire frame is stored.RSR is a 12 bit shift register with 8 bit data and extra 4bits error logic.

Now if the Receiver Hold Register (RHR) is empty it sends signal to RSR so that only the data bits from RSR goes to RHR which is an 8 bit register with discarding the extra 4 bits which are in error logic. The remaining bits in the RSR are used by the error logic block. Then, if receiver FIFO is empty without any data contained in it, it then send the signal to RHR so that the data bits goes to FIFO. When RD signal is asserted the data is available in parallel form on the RXOUT0-RXOUT7 pins (0-7) bits are shown. The status register is implemented with flags for error logic operations performed on the received data. The error logic block handles 4 types of errors, Parity error (PE), Frame error (FE), Overrun error (OE), Break error (BE). If the received parity does not match with the parity generated. From data bits, PE bit will be set which indicates that parity error occurred. If receiver fails to detect correct stop bit or when 4 samples do not match frame error occurs and FE bit is set. If the receiver FIFO is full and other data arrives at, RHR overrun error occurs and OE bit is set. If the RXIN pin is held low for long time than the frame time then there is a break in received data and break error occurs and BE bit is set.

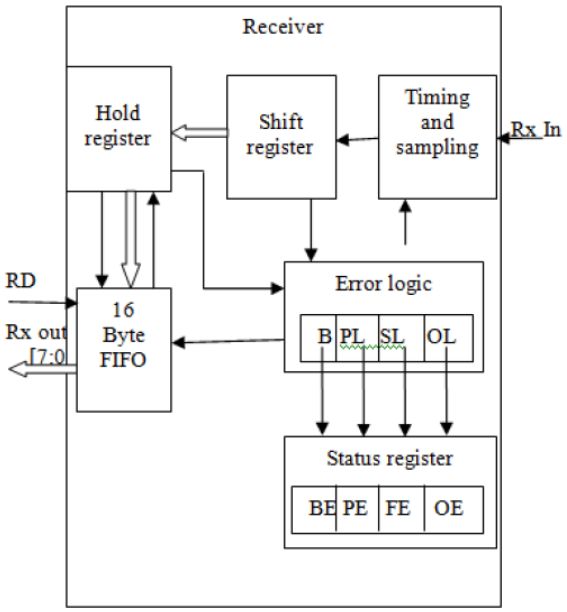

Fig6: UART Receiver

III. AUTOMATIC BAUD RATE DETECTION

In this section, it describes the method to find automatic baud rate. Basic UART module consist of transmitter, receiver, FIFO ,baud rate generator.

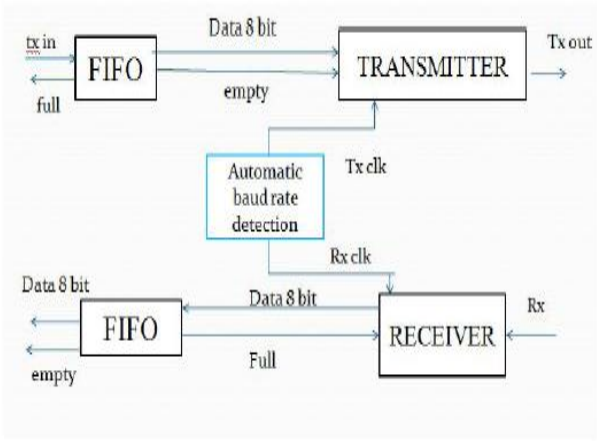

Fig7: Automatic Baud rate detection

FIFO:

FIFO is a special type of buffer. The name FIFO stands for first in first out and means that the data written into the buffer first comes out of it first. There are other kinds of buffers like the LIFO (last in

first out), often called a stack memory, and the shared memory. The choice of buffer architecture depends on the application to be solved. FIFOs can be implemented with software or hardware.

The choice between software and a hardware solution depends on the application and the features desired. When requirements change, a software FIFO easily can be adapted to them by modifying its program, while a hardware FIFO may demand a new board layout. Software is more flexible than hardware. The advantage of the hardware FIFOs shows in their speed. FIFO is implemented as a queue structure and it has a fixed length. If FIFO is empty or is not fully filled then only the data can be written into it .If FIFO is full ,it sends a signal “FULL” to the transmitter and receiver. Otherwise it sends “EMPTY” to both transmitter and receiver end.

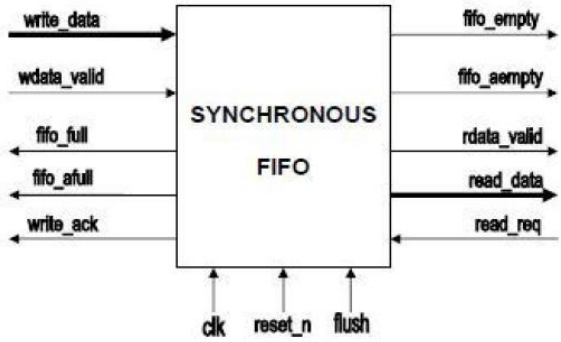

Fig 8: FIFO General Blocks

Automatic baud rate generator:

UART is operating with fixed baud rate for the transmitter. As the baud rate of the transmitter (master) changes the receiver (slave) cannot adjust with the master automatically. It is also time consuming..Automatic detection is useful for establishing communication link between two devices. The slave device will be able to detect he baud rate of the master controller and adjust accordingly.

The most commonly used number of data bits of a serial connection is eight, which corresponds to a byte. When a regular ASCII code is used in communication, only seven LSBs are used and the MSB is 0.If the UART is configured as 8 data bits,1 stop bit ,and no parity bit ,the received data is in the form of 0-dddd-ddd-0-1, in which d is a data bit and can be 0 or 1. Assume that there is sufficient time between the first word and subsequent transmissions. In this scheme, the transmitting system first sends an ASCII code for rate detection and then resumes normal operation afterward. The receiving subsystem uses the first word to determine a baud rate and then uses this rate for the baud rate generator for the remaining transmission. Assume that the UART configuration is 8 data bits, 1 stop bit, and no parity bit, and the baud rate can be 4800, 9600, or 19,200 baud. The revised UART receiver should have two operation modes. It is initially in the "detection mode" and waits for the first word. After the word is received and the baud rate is determined, the receiver enters "normal mode" and the UART operates in a regular fashion.

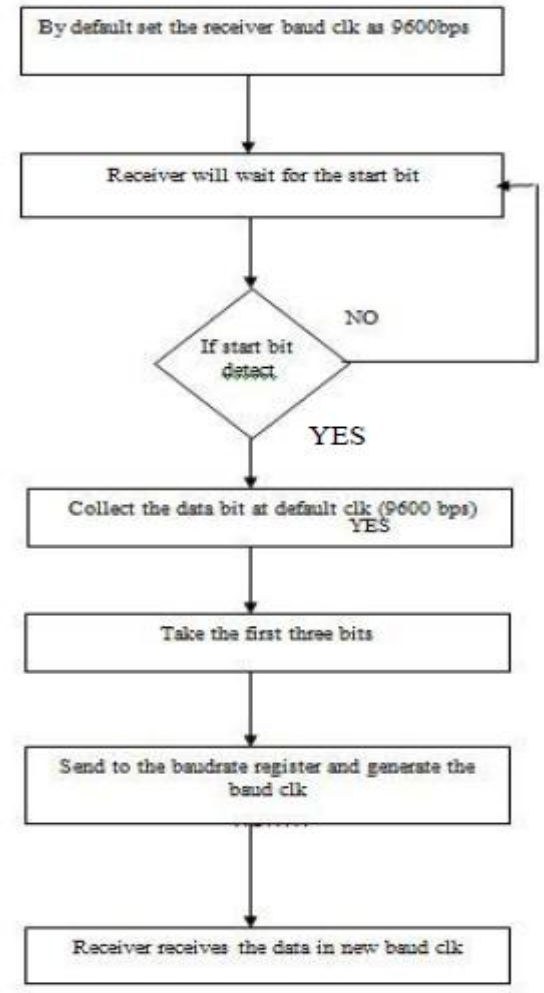

Fig9: Flow diagram of Automatic baud rate generator

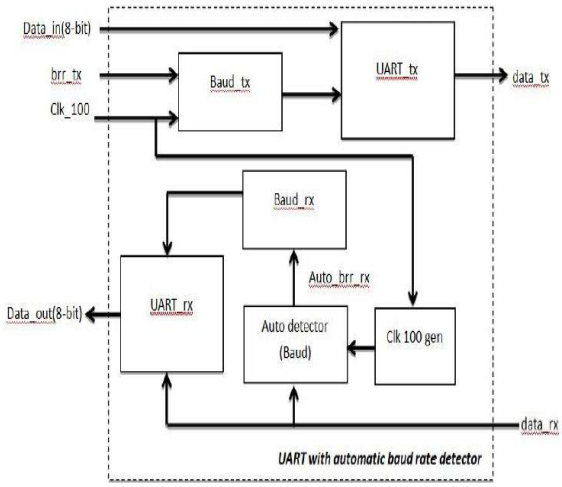

Fig10: Complete UART module

Simulation Results:

The implementation of the function in vhdl coding and verilog coding and simulation of the design are done in Xilinx model sim 12.3.the baud rate set is 9600bps.the word length of the data used here is 8 bit. The comparison is shown here for the already existing theory which is present and the proposed theory.

Simulation result of top module:

The result shows the data transmitted is received without any error corrections is checked in the form of reference output and tested output.

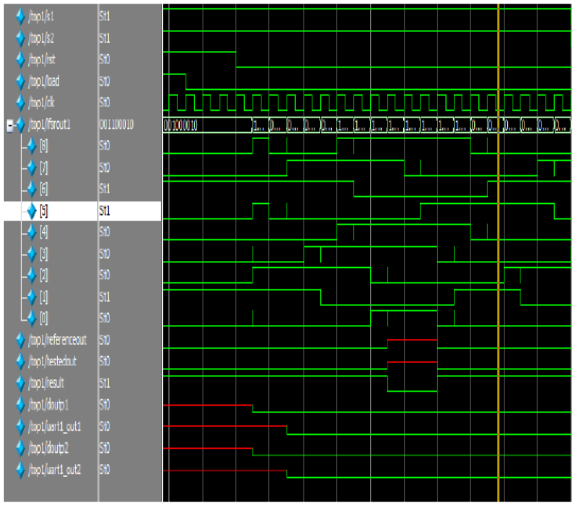

Fig11: UART with BIST Result

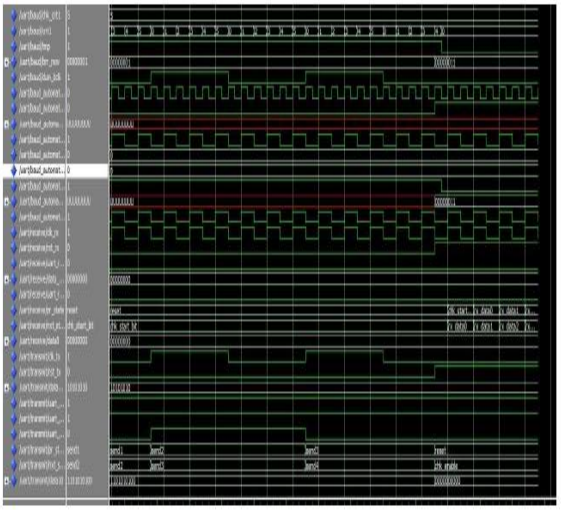

Fig12: UART Automatic baud rate generator Result

Universal asynchronous receiver transmitter, (UART) is an integrated circuit used for serial communication over a computer or peripheral device serial port with fixed baud rate. Here we introduce the concept of automatic baud rate detection. so when the transmitter changes the baud rate the receiver can adjust automatically and it reduces the delay for the reception of data than the fixed baud rate.

Device Utilization Summary (estimated values)			[-]
Logic Utilization	Used	Available	Utilization
Number of Slices	48	4656	1%
Number of Slice Flip Flops	67	9312	0%
Number of 4 input LUTs	75	9312	0%
Number of bonded IOBs	17	232	7%
Number of GCLKs	1	24	4%

Fig13: Device Utilization Summary

IV. CONCLUSIONS

In many cases, serial is a better The building design of UART with BIST method that backings the 8-bit information word length for the serial correspondence of information with the status register to identify the mistakes created and gives the right transmission of information at data and getting at the yield. By utilizing the BIST method as a part of UART serial correspondence we can lessen the prerequisites of the analyzer capacities and the ventures in it. The LFSR which delivers the pseudo irregular test designs as information to the transmitter to give better blame scope to the UART module. Because of the expansion of the circuit by including BIST idea also we had increment in outline time and equipment use however by the decrease of

the expense and great business sector opportunities we can cover the issue. UART is an incorporated circuit utilized for serial correspondence more than a PC or fringe gadget serial port with settled baud rate. Here we present the idea of programmed baud rate location. so when the transmitter changes the baud rate the beneficiary can change naturally and it diminishes the postponement for the gathering of information than the settled baud rate.

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