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RESEARCH ARTICLE

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FPGA APPROACH TO LDPC CODE IMPLEMENTATION

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ABSTRACT

Low-density parity-check (LDPC) codes can be measured as serious competitors to turbo codes in requisites of performance and intricacy. For making the efficient use of available limited bandwidth code modulation is the good competitor on comparing it with some other. Our central goal is in the direction to realize LDPC scheme within VLSI technologies. Under this approach encoder of LDPC implementation is done by using Shift register based proposes to reduce intricacy. In this paper performance parameters are studied and then find variation in SNR performance. LDPC performance is taken using Phase Shift Keying technique in AWGN environment. Eventually we compare LDPC system with FPGA implemented system performance with the SNR performance.

Keywords: Belief propagation, LDPC, BPSK, AWGN, FPGA.

INTRODUCTION

Low-density parity-check codes, introduced by Gallager in 1962 [1] and their performance under "belief propagation" decoding, has been the theme of recent experimentation and study [2, 3, 4, 5]. The interest in these codes stems from their near Shannon limit performance the connection between transmitter and receiver is established through communication channel. The communication channel take place through wire as well as wireless medium or can use optical channels. The other medium such as optical disc, magnetic tapes and discs etc. can also be called as communication channel because they can also carry data through them.

Received data steadfastness depends on the medium of channel used and external noise too. Noise effect is very dominant in medium and possibly will introduced somber error in transmitted data. According to Shannon's theorem if data rate is less than that of channel capacity, data could be transmitted unfailingly. In this theorem a sequence of codes less than the channel capacity have a capability as the code length goes to infinity [6].

Error correcting and error detecting also plays a foremost role ever since they were discovered.

This technique achieved by just adding a spare symbol called redundant symbols to the original data. Prior to these ECC if any error is occurred during the reception of transmitted signal data need to retransmitted, this approach adds delay, waste system throughput and increases cost. ECC are really helpful for long distance communication for instance satellite communication. With the increased capacity of a computer and the development of relevant theories such as propagation algorithm and turbo codes, LDPC codes were rediscovered by Mackay (*et al.* 1995) [7].

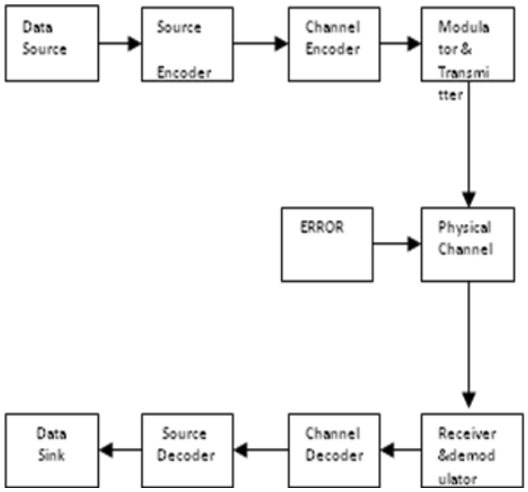


Figure 1 Basic communication channel

Some procedures for constructing good LDPC codes can be brief into two chief classes: random and structural constructions. Normally, for long code lengths, random constructions [8], [9] of irregular LDPC codes have been shown to closely approach the theoretical capacity limits for the additive white Gaussian noise (AWGN) channel.

Due to advancement of VLSI technologies, it is possible to manufacture very high speed embedded circuits. Such circuits are used in today's communication sector. Even ULSI technologies are use in various applications nowadays. High speed computer and powerful software design tools are available. In figure 1 a communication channel system was shown in which data is move between source and destination.

VLSI IMPLEMENTATION

LDPC Encoder

The LDPC encoder deals with the production of message matrix with generator matrix. The process becomes cumbersome when encoding with higher matrix rates. Following are the steps foe encoding:

Step I

Parity matrix **H** is selected from circulant encoding and may give in the following form

$$\mathbf{H = [-P_T; I_{n-k}]}$$

Step 2

Generator matrix **G** is generated from the parity matrix as:

$$\mathbf{G = [I_K; P]}$$

Step 3

Under this step code word 'c' for message 'm' will be

$$\mathbf{c = mG}$$

Generally the H matrix is of the form of 2048x4096. Then G matrix will be of the form 2048x4096, but as we have to write for each link between check node and variable node, their practical implementation is a very tedious task. Hence here we take a small matrix of 16x32 and by using this technique we can implement big matrix for any greater size.

The H matrix and G matrix used for VHDL implementation is given in sparse form:

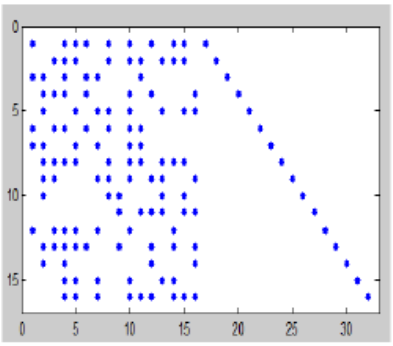


Figure 2: H matrix sparse matrix

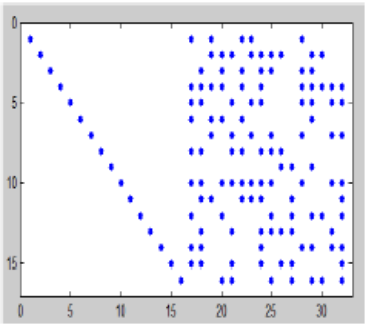


Figure 3: G matrix sparse matrix

As earlier mention that here we take a generator matrix of 16× 32 dimension so the message will be of 16 bits and another multiplication matrix between message stream and generator matrix. For the implementation purpose here we have taken a *Xilinx XC3S500E FPGA* (Spartan 3E) board.

Let us familiar with the implementation of LDPC encoder:

Step 1: For storing the generator matrix we have taken a required numbers of registers. Here in our case we have 16X32 dimension matrix so that we required 16 bits and 32 bits register.

Step 2 : Write the matrix multiplication between message matrix (1X16) and generator matrix which is a combination of 'AND' & 'OR' gates.

Step 3 : Now under this step we transmit the message (m) bits through "Test Bench".

Step 4 : The output is now given out for transmission through the AWGN channel.

Encoder top level schematic:

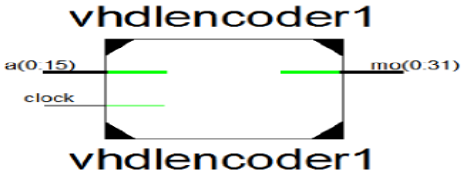


Figure 4: Top level schematic for encoder

I/O Bus in Encoder:

a (0:15): Message Input -16 bit

clock: Clock Signal - 1 bit

mo: Encoded Signal -32 bit

Encoder RTL schematic:

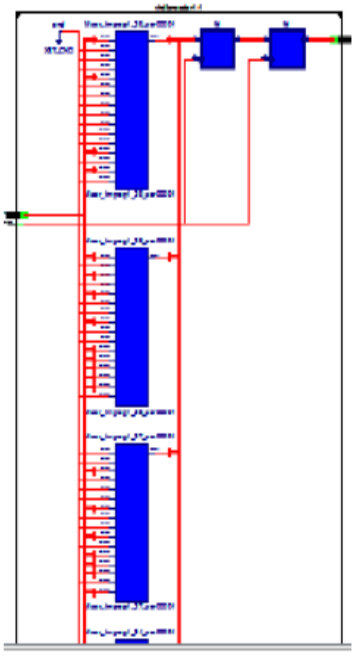


Figure 5: Encoder RTL schematic

Device Utilization:

The encoder is implemented on *Xilinx XC3S500E FPGA* (Spartan 3E), the device utilization are as follows:

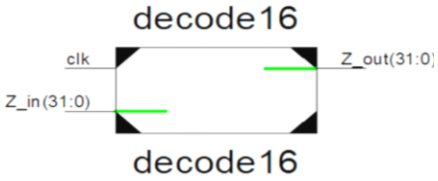
S.No.	Device Utilization			
	Logic utilization	Used	Available	Utilization
1.	Number of slices	30	960	3%
2.	Number of slice Flip Flop	47	1920	2%
3.	Number of 4 input LUT's	53	1920	2%
4.	Number of bonded IOB's	49	56	74%
5.	Number of GCLK's	1	24	4%

Table 1: Device utilization of Encoder in Spartan 3E

VHDL IMPLEMENTATION OF LDPC DECODER

In lieu of keeping the values and their estimated value through variable and check node we practice the look up table (LUT). We have employed the decoder using XilinxVirtex-4 ML401 as the board.

Top Level Schematic of Decoder:



I/O Bus in Decoder:

Z_in (31:0): Message Input -32 bit
clock: Clock Signal - 1 bit
Z_out: Decoded Signal -32 bit

Figure 6: Top Level Schematic of Decoder

RTL Schematic of the Decoder:

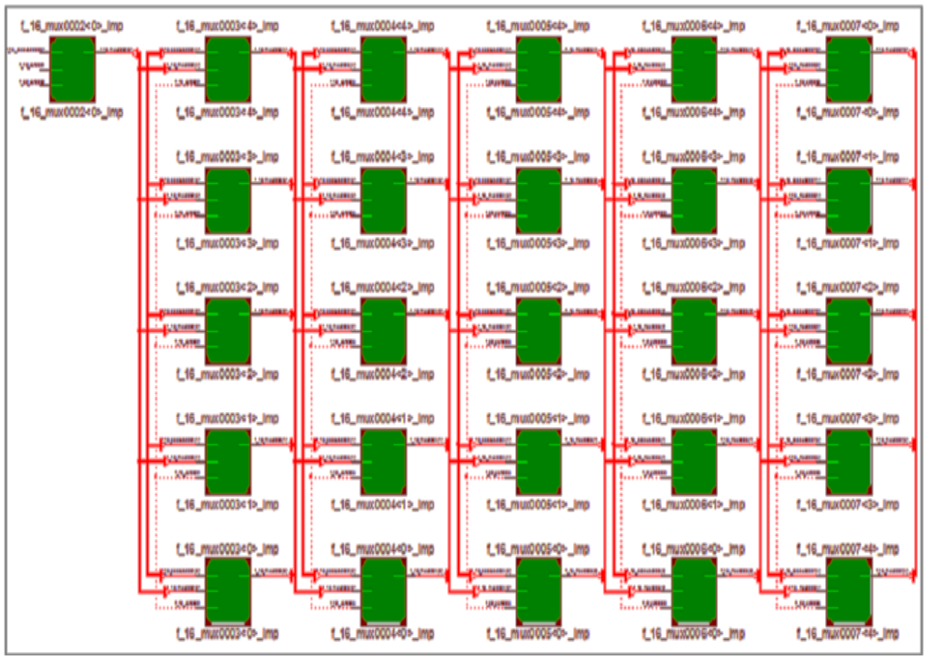


Figure 7: Decoder RTL schematic enlarged

Device Utilization:

DEVICE UTILIZATION ESTIMATED SUMMARY

LOGIC UTILIZATION	USED	AVAILABLE	UTILIZATION
NUMBER OF SLICES	100	5472	1%
NUMBER OF SLICE FLIP FLOPS	40	10944	0%
NUMBER OF 4 INPUT LUT'S	181	10944	1%
NUMBRER OF BONDED IOB'S	43	240	17%
NUMBER OF GCLK'S	1	32	3%

Table 2: Device Utilization estimated summary

RESULT

The performance of the system is considered first under Matlab. The same H matrix and G matrix used in this encoder/decoder is first tested under Matlab environment .Then it is checked by means of taking some message bits and transmitting it through Test BenchWave form BER vs. SNR curve for encoder and decoder is as given below.

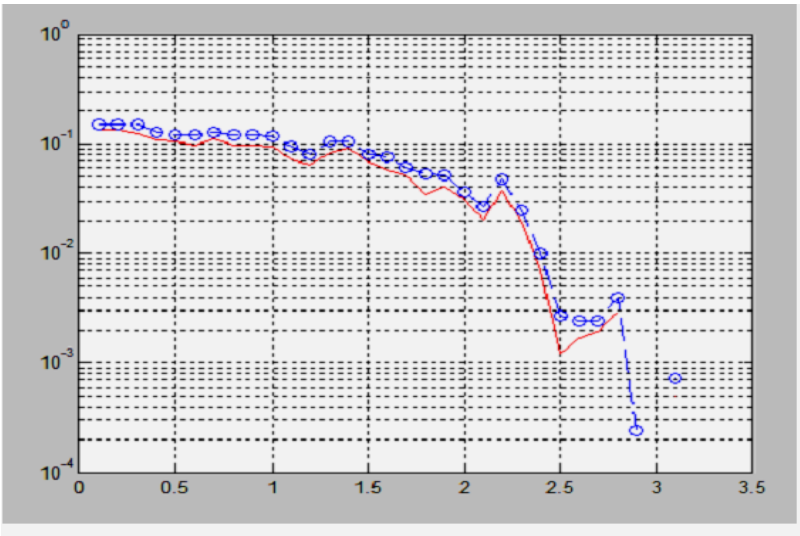


Figure 8.1: Encoder/Decoder SNR for H matrix

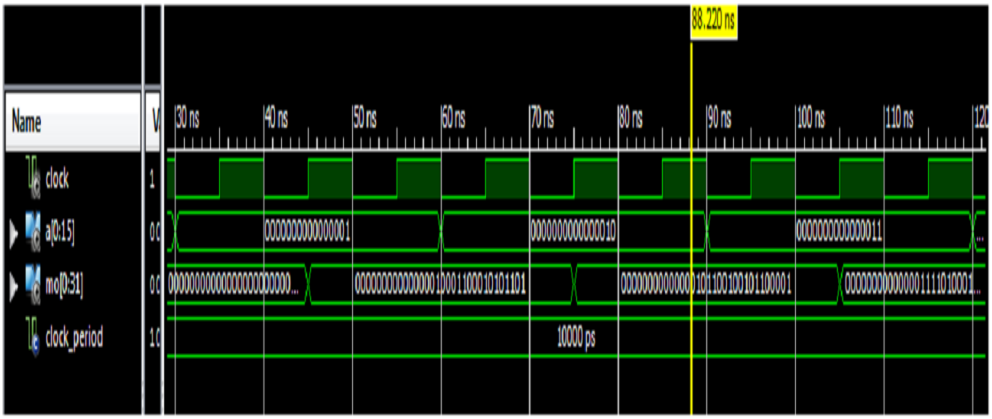


Figure 8.2: Test bench for Encoder circuit

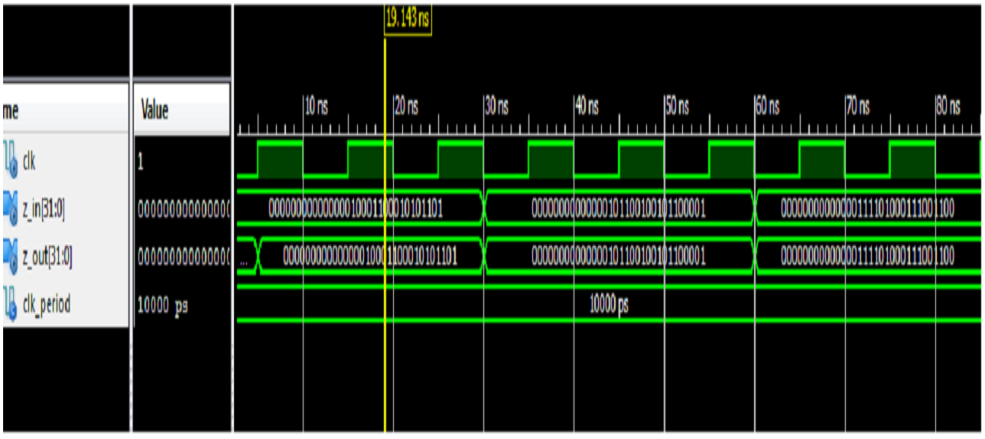


Figure 8.3: Test bench for Decoder circuit

FUTURE WORK

An assortment of modulation proposal for instance **Wi-Max**(802.3) wireless communication standard,**DVB-S2**,OFDM; LDPC code set up a superior correcting code and it's presentation is next to that of Shannon's' limit which put together it in best runner. The realization of OFDM scheme in support with LDPC is our chief objective.Every now and then LDPC take up with additional Block correction codes for enhanced response in collaboration with RS code. In upcoming communication techniques like 5G OFDM (Orthogonal Frequency Division Multiplex) is going to be a good competitor. In addition with this approach error correcting coeds play an imperative role. OFDM experience a quandary like ISI (Inter Symbol Interference)**,** PAPR (Peak to Average Power Ratio) and so forth, therefore by exploiting LDPC we resolve these quandary in OFDM and then progress to realization. The combined LDPC and DCT with companding scheme for the reduction of the PAPR of OFDM signals. This technique can also be extended to MIMO system with adaptive modulation scheme.

By using the channel LDPC coding with diversity combining technique for instance MRC/SC, the BER performance of system is improved. For transmitting multipath signal by controlling the effect of channel fading OFDM has a awfully ample scope in transmission of data. In outlook it is also feasible to design a channel using different coding and decoding techniques which confiscate the consequence of Multipath fading in superior than these channels.

CONCLUSION

We have considered various encoding and decoding schemes algorithms and amid which LDPC code is develop a worthy block error correcting code. The supreme imperative feature is its performance in error atmosphere and performance was closer to that of Shannon's limit. We checked the LDPC performance by means of BPSK system in Matlab and implement this using FPGA VLSI technology. Performance be governed on some additional parameters like as matrix dimension regularity etc.

In log domain Sum-Product Algorithm come to be a dominate competitor and spectacle good error performance. Decoder performance was also found closer to Shannon's limit and was calculated including Min-Sum and message passing technique. Implementation of encoder and decoder was finished by using Spartan 3E and Virtex 4board.

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