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RESEARCH ARTICLE

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A SURVEY ON ADAPTIVE EDGE-ENHANCED COLOR INTERPOLATION PROCESSOR FOR VLSI ARCHITECTURE

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ABSTRACT

The digital cameras are developed by Charge Coupled Device (CCD) or Complementary Metal Oxide Semiconductor (CMOS) image sensor that can capture images by Color Filter Array (CFA) technique. A CFA used in digital camera is a mosaic of spectrally selective filters, which allow only one color component to be sensed at each pixel. The missing two components of each pixel have to be estimated by methods known as Demosaicing. In this survey, different types of interpolation algorithm and their hardware architecture have been analyzed and compared. The algorithms are implemented for different types of field programmable gate array (FPGA) and/or by different types of complementary metal oxide semiconductor (CMOS) technologies like TSMC 0.18 and TSMC 0.13. Here, we propose a low complexity adaptive edge-enhanced color interpolation algorithm for the VLSI implementation in real time video applications. The goal of this proposed work is to reduce computational complexity by reducing the number of components used for interpolation. This novel algorithm consists of an edge detector, an anisotropic weighting model and a filter based compensator. This proposed work is tries to reduce the number of line buffers and combinational elements such as adder and multiplexer of the existing architecture. In addition, the hardware cost was reduced by using hardware sharing and reconfigurable techniques.

Key words- Camera, Charge coupled device (CCD), Demosaicing, Color filter array (CFA), Edge detector, Interpolation, FPGA.

INTRODUCTION

Digital cameras have become popular and many people are choosing to take their pictures with digital cameras instead of film cameras. When a digital image is recorded, the camera needs to perform a significant amount of processing to provide the user a viewable image. This processing includes white balance adjustment, gamma correction, compression and more. A very important part of this image processing chain is color filter array interpolation or demosaicing. A color image requires at least three color samples at each pixel location. A camera would need three separate sensors to make these measurements. To reduce the size and cost, many cameras use a single sensor array with a color filter array. The color filter array allows only one part of the spectrum to pass to the sensor so that only one color is measured at each pixel. This means the camera must estimate the missing two color values at each pixel. This process is known as demosaicing. The most frequently used color filter array pattern is the Bayer CFA pattern shown in figure 1.

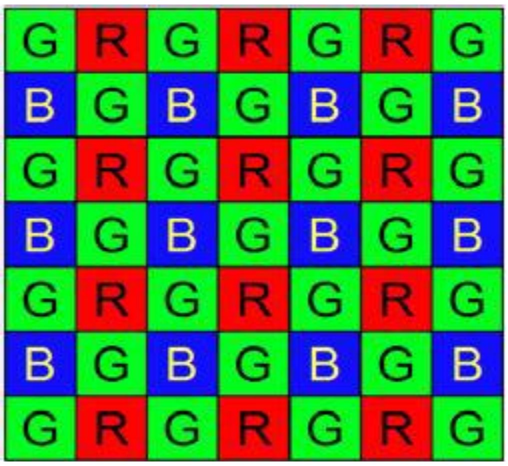

Figure 1: Bayer CFA pattern

In the above figure, half of the pixels are allocated to the green color; other half is shared by the red and blue color. The green image is measure at higher sampling rate because the peak sensitivity of the human visual system lies in the medium wavelength, corresponding to the green portion of the spectrum. Many efficient high quality algorithms have been proposed for reconstructing the full RGB color from CFA images. But these algorithms have the characteristics of high complexity and high memory requirement. Furthermore, these algorithms are not easy to be realized using VLSI technique. For this reason, the VLSI architecture of low complexity and low memory requirement color interpolation algorithms were conducted.

COLOR DEMOSAICING METHODS

Several demosaicing methods has been published in the past decade. Demosaicing methods are divided into three groups:

1) Heuristic approaches
2) Restoration techniques
3) Image formation modeling

Heuristic approaches do not try to solve a mathematically defined problem, but they are based on reasonable assumptions about color images. Heuristic approaches are spatially adaptive, and they may exploit correlation among the color channels.

The second group of algorithms makes some assumptions about the inter-channel correlations, and solves a mathematical problem based on those assumptions.

The last group of methods models the image formation process and formulates the demosaicing problem based on this model.

Low power High quality Color Interpolation Processor for CCD Camera [10]

VLSI implementation of low power high quality color interpolation is proposed for CCD camera. This method provides a color interpolation technique for a single-chip charge coupled device (CCD) with color filter array format. The performance of this design was improved by a pipeline schedule and time sharing technique. Although the local gain that is obtained by the edge direction weighting information, it can efficiently improve the quality of interpolated images. Based on this algorithm, we arrange a suitable timing schedule to compute various color components for real time chip implementation using a parallel architecture. It is necessary to use two division and three multiplication operations to obtain the edge direction weighting and local gain information. Figure 2 shows the interface of the color interpolation processor.

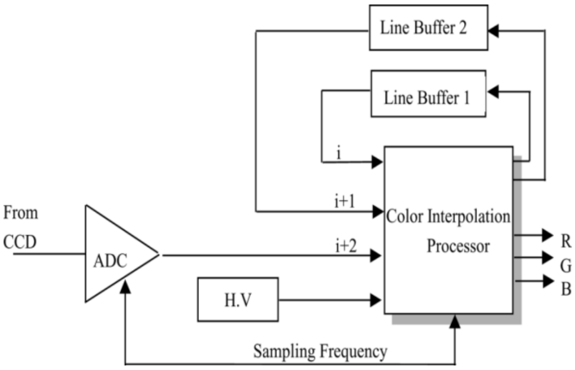

Figure 2: Interface of the color interpolation processor

In this figure, the CCD signal is sampled with an analog/ digital converter (ADC), and then the sampling data is sent to a color interpolation processor. Meanwhile the color interpolation processor reads the vertical and horizontal synchronous signals to control the operators. The color interpolation algorithm also employs three scanning lines, so real time implementation requires two line buffers. The line buffers are used to store the scanning lines.

An Area Efficient Color Demosaicing Scheme [11]

VLSI implementation of area efficient demosaicing scheme is proposed for digital still camera (DSC). This design improved the quality of interpolated images by using edge information and inter- channel correlations. By using pipeline architecture, the performance was greatly improved. Since the parameters of the edge-information and inter-channel correlations were divided by 2, 4, or 8, it is unnecessary to use any divider to realize this design. With this implementation technique, the chip area significantly reduced. The reconstructed pixels are interpolated along the edge instead of across the edge, so, may obtain better image quality. Figure 3 shows the block diagram of demosaicing chip. The VLSI architecture consist of four main parts: the interpolating unit, the line buffer, the register bank and the control unit. The interpolating unit performs the interpolation process row by row to generate the missing R, G or B components of each pixel. A line buffer is used to store the pixel values of one row in the image. The register bank is employed to store the neighboring pixel values temporally and provide the needed data to the interpolating unit. The control unit provides the control signals to other units and handles the whole interpolation flow.

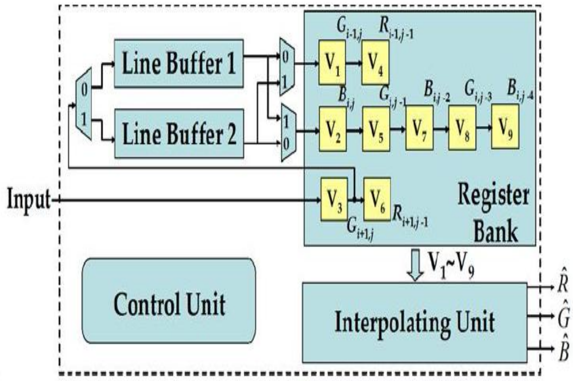

Figure 3: Block diagram of demosaicing chip

Adaptive homogeneity directed demosaicing algorithm [6]

The demosaicing algorithm estimates missing pixels by interpolating in the direction with fewer color artifacts. To identify three inherent problems often associated with directional interpolation approach to demosaicing algorithms: misguidance color artifacts, interpolation color artifacts, and aliasing. The level of misguidance color artifacts present in two images can be compared using metric neighborhood modeling. The aliasing problem is solved by applying filter bank techniques to directional interpolation. The interpolation artifacts are reduced using a nonlinear iterative procedure.

Demosaicing algorithm with a directionality selection approach suffers from two types of color artifacts. The first type is called misguidance color artifact. The misguidance occurs when the direction of interpolation is erroneously selected. The second type of color artifact is associated with limitations in the interpolation. That is, even with a perfect directional selector, the interpolation algorithm may not reconstruct the color image perfectly. Interpolation artifacts are reduced using iterative algorithm. The following iterative procedure, performed m times, suppresses small variation in color while preserving edges:

repeat _m_ times

1. R = median (R-G) + G
2. B = median (B-G) + G
3. G = ½ (median (G-R) + median (G-B) + R + B)

end _ repeat.

Wavelet based color filter array demoasicing [17]

To employ the higher spatial resolution of the luminance image, by merging it with the interpolated color image. For this merging, multiresolution techniques using the wavelet transform. Employ the wavelet transform for the merging of an interpolated luminance image with an interpolated color image, where the conventional interpolation techniques are applied. In a first step, a luminance image is formed. This can be done in one of the conventional ways (bilinear interpolation of the green pixels as in the Bayer reconstruction, the alternative Bayer reconstruction or the gradient reconstruction). Also the red, blue, and green component images are interpolated in a conventional ways. Then the luminance image and each band of the RGB image is wavelet transformed separately. Two merging rules are investigated: the 'replace' rule replaces the coefficients from the color band by the coefficients from the luminance image. The 'max' rule replaces the coefficients from the color band by the maximum of the coefficients from the luminance and the color band. Finally the obtained color wavelet coefficients are inversely wavelet transformed to obtain the demosaicked RGB image.

Adaptive CFA demosaicing using Directional spatial and spectral correlations [14]

To develop a new and improved CFA demosaicing method for producing high quality color images from CFA samples. This method consists of two successive steps:

1) Interpolation step
2) Post processing step

An interpolation step estimating the missing color values by exploiting spatial and spectral correlations among neighboring pixels in different directions, and a post processing step suppressing noticeable artifacts by using adaptive mean filtering. The interpolation step fills in missing color values in sequentially, the green plane is the first to be fully populated and (once fully populated) used to assist the subsequent red and blue plane interpolation. Each missing color value is interpolated by properly combining the estimates obtained from four interpolation directions which are defined based on the four nearest CFA samples of the same color. The estimates from one particular direction is obtained by exploiting the spectral correlations along that directions, the correlation that states that the difference between the green and red/blue values within a local neighborhood are well correlated with constant offsets. The post processing step aims to suppress visible artifacts residing in the demosaicked images obtained from the interpolation step. There are two main types of demosaicking artifacts, namely false colors and zipper effect. The false colors are those artifacts corresponding to noticeable color errors as compared to the non-mosaicked original image. The zipper effect refers to abrupt or unnatural changes in color or intensity between neighboring pixels, manifesting as an "on-off" pattern.

PROPOSED METHOD

Here, a low complexity adaptive edge enhanced color interpolation algorithm is proposed for the VLSI implementation in real time video applications. The proposed novel algorithm consists of an edge detector, an anisotropic weighting model and a filter-based compensator. The anisotropic weighting model is designed to catch more information in horizontal direction than vertical directions. A low complexity edge detector is created to enhance the edge information in the images. It used only addition, subtraction, and absolute operations to obtain the edge information. The hardware cost of the edge detector is much less than the previous designs such as [8] and [10], which utilize dividers and multipliers to obtain the edge and gain information. The filter-based compensation methodology includes a Laplacian and spatial sharpening filters which are developed to improve the edge information and reduce the blurring effect. The hardware cost is reduced by using hardware sharing and reconfigurable techniques. Compared with previous low complexity techniques, this work reduces the gate counts or power consumption, also improves the average CPSNR quality.

CONCLUSION

In this paper different types of interpolation algorithm and their hardware architectures are discussed. Also a novel color interpolation algorithm is proposed to develop low cost, low power, high performance, and high quality color interpolation processor for real time video applications. This algorithm consists of an anisotropic weighting model, an edge detector, and filter-based compensation methods which are used to reduce the memory requirements and improve the quality of images. The number of arithmetic elements in proposed architecture is much less than the other interpolation methods.

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