

REVIEW ARTICLE



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SEVEN-LEVEL INVERTER WITH NOVEL PULSE WIDTH MODULATION TECHNIQUE FOR PV APPLICATIONS

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ABSTRACT

This paper proposes a single-phase seven-level inverter for grid-connected photovoltaic systems, with a novel pulse width modulated (PWM) control scheme. Three reference signals that are identical to each other with an offset that is equivalent to the amplitude of the triangular carrier signal were used to generate the PWM signals. The inverter is capable of producing seven levels of output-voltage levels (V_{dc} , $2V_{dc}/3$, $V_{dc}/3$, 0 , $-V_{dc}/3$, $-2V_{dc}/3$, $-V_{dc}$) from the dc supply voltage. A digital proportional–integral current-control algorithm was implemented in a TMS320F2812 DSP to keep the current injected into the grid sinusoidal. The proposed system was verified through simulation and implemented in a prototype.

Key Words—Grid connected, modulation index, multilevel inverter, photovoltaic (PV) system, pulse width-modulated (PWM), total harmonic distortion (THD).

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INTRODUCTION

The ever-increasing energy consumption, fossil fuels' soaring costs and exhaustible nature, and worsening global environment have created a booming interest in renewable energy generation systems, one of which is photovoltaic. Such a system generates electricity by converting the Sun's energy directly into electricity. Photovoltaic-generated energy can be delivered to power system networks through grid-connected inverters. A single-phase grid-connected inverter is usually used for

residential or low-power applications of power ranges that are less than 10 kW [1]. Types of single-phase grid-connected inverters have been investigated [2]. A common topology of this inverter is full-bridge three-level. The three-level inverter can satisfy specifications through its very high switching, but it could also unfortunately increase switching losses, acoustic noise, and level of interference to other equipment. Improving its output waveform reduces its harmonic content and, hence, also the

size of the filter used and the level of electromagnetic interference (EMI) generated by the inverter's switching operation[3]. Multilevel inverters are promising; they have nearly sinusoidal output-voltage waveforms, output current with better harmonic profile, less stressing of electronic components owing to decreased voltages, switching losses that are lower than those of conventional two-level inverters, a smaller filter size, and lower EMI, all of which make them cheaper, lighter, and more compact [3], [4]. Various topologies for multilevel inverters have been proposed over the

years. Common ones are diode-clamped [5]– [10], flying capacitor or multi cell [11]–[17], cascaded H-bridge[18]–[24], and modified H-bridge multilevel [25]–[29]. This paper recounts the development of a novel modified H-bridge single-phase multilevel inverter that has two diode embedded bidirectional switches and a novel pulse width modulated (PWM) technique. The topology was applied to a grid connected photovoltaic system with considerations for a maximum-power-point tracker (MPPT) and a current-control algorithm.

II. PROPOSED MULTILEVEL INVERTER TOPOLOGY

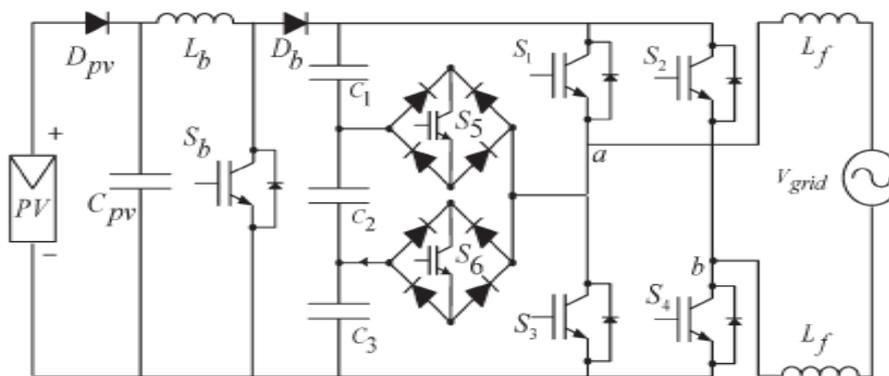


Fig:1 Proposed single-phase seven-level grid-connected inverter for photo voltaic system

The proposed single-phase seven-level inverter was developed from the five-level inverter in [25]–[29]. It comprises a single-phase conventional H-bridge inverter, two bidirectional switches, and a capacitor voltage divider formed by C_1 , C_2 , and C_3 , as shown in Fig. 1. The modified H-bridge topology is significantly advantageous over other topologies, i.e., less power switch, power diodes, and less capacitors for inverters of the same number of levels. photovoltaic (PV) arrays were connected to the inverter via a dc–dc boost converter. The power generated by the inverter is to be delivered to the power network, so the utility grid, rather than a load, was used. The dc–dc boost converter was required because the PV arrays had a voltage that was lower than the grid voltage. High dc bus voltages are necessary to ensure that power flows from the PV arrays to the grid. A filtering inductance L_f was used to filter the current injected into the grid. Proper switching of the inverter can produce seven output-voltage levels (V_{dc} , $2V_{dc}/3$, $V_{dc}/3$,

0 , $-V_{dc}$, $-2V_{dc}/3$, $-V_{dc}/3$) from the dc supply voltage. The proposed inverter's operation can be divided into seven switching states, as shown in Fig. 2(a)–(g). Fig. 2(a), (d), and (g) shows a conventional inverter's operational states in sequence, while Fig. 2(b), (c), (e), and (f) shows additional states in the proposed inverter synthesizing one- and two-third levels of the dc-bus voltage. The required seven levels of output voltage were generated as follows.

Maximum positive output (V_{dc}): S_1 is ON, connecting the load positive terminal to V_{dc} , and S_4 is ON, connecting the load negative terminal to ground. All other controlled switches are OFF; the voltage applied to the load terminals is V_{dc} . Fig. 2(a) shows the current paths that are active at this stage. Two-third positive output ($2V_{dc}/3$): The bidirectional switch S_5 is ON, connecting the load positive terminal, and S_4 is ON, connecting the load negative terminal to ground. All other controlled switches are OFF; the voltage applied to the load

terminals is $2V_{dc}/3$. Fig. 2(b) shows the current paths that are active at this stage.

One-third positive output ($V_{dc}/3$): The bidirectional switch S_6 is ON, connecting the load positive terminal, and S_4 is ON, connecting the load negative terminal to ground. All other controlled switches are OFF; the voltage applied to the load terminals is $V_{dc}/3$. Fig. 2(c) shows the current paths that are active at this stage.

Zero output: This level can be produced by two switching combinations; switches S_3 and S_4 are ON, or S_1 and S_2 are ON, and all other controlled switches are OFF; terminal ab is a short circuit, and

the voltage applied to the load terminals is zero. Fig. 2(d) shows the current paths that are active at this stage.

One-third negative output ($-V_{dc}/3$): The bidirectional switch S_5 is ON, connecting the load positive terminal, and S_2 is ON, connecting the load negative terminal to V_{dc} . All other controlled switches are OFF; the voltage applied to the load terminals is $-V_{dc}/3$. Fig. 2(e) shows the current paths that are active at this stage.

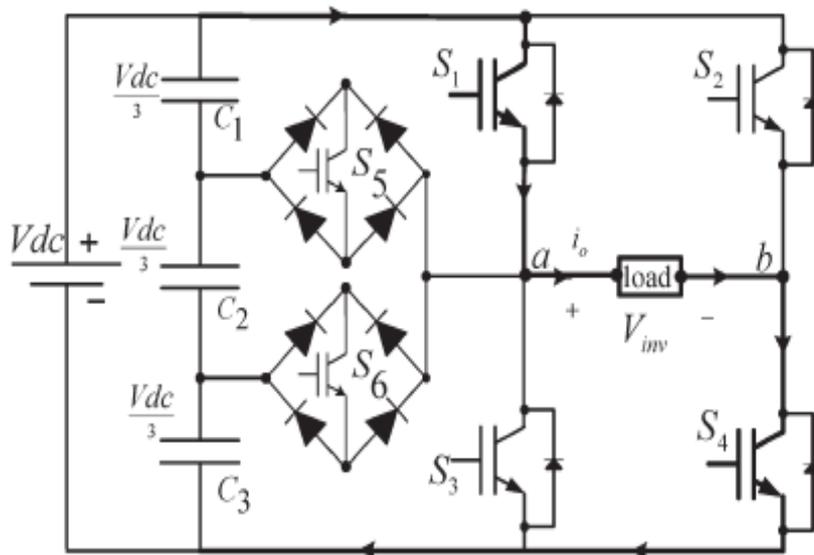


Fig: 2 (a) Switching combination required to generate the output voltage $V_{ab} = V_{dc}$

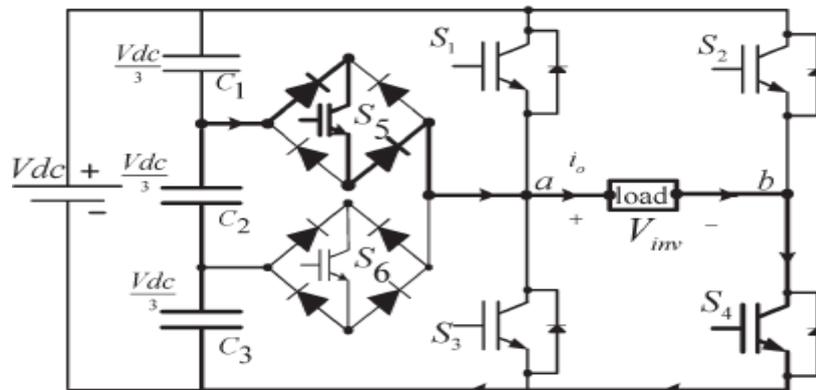


Fig: 2 (b) Switching combination required to generate the output voltage $V_{ab} = 2V_{dc}/3$

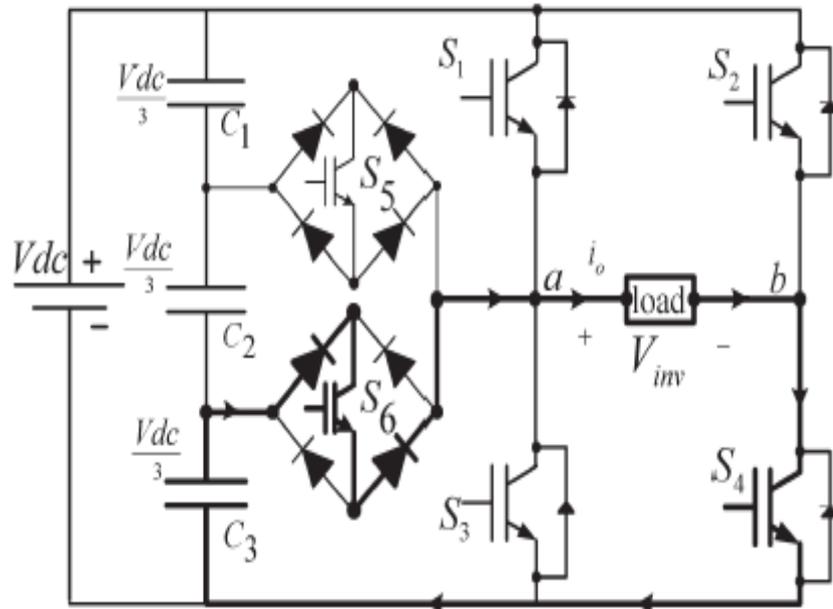


Fig: 2 (c) Switching combination required to generate the output voltage $V_{ab} = V_{dc}/3$

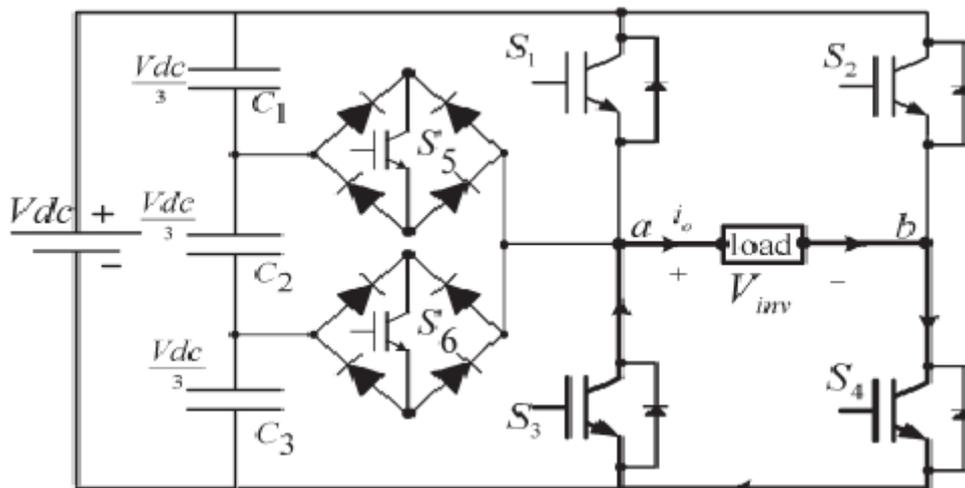


Fig: 2 (d) Switching combination required to generate the output voltage $V_{ab} = 0$

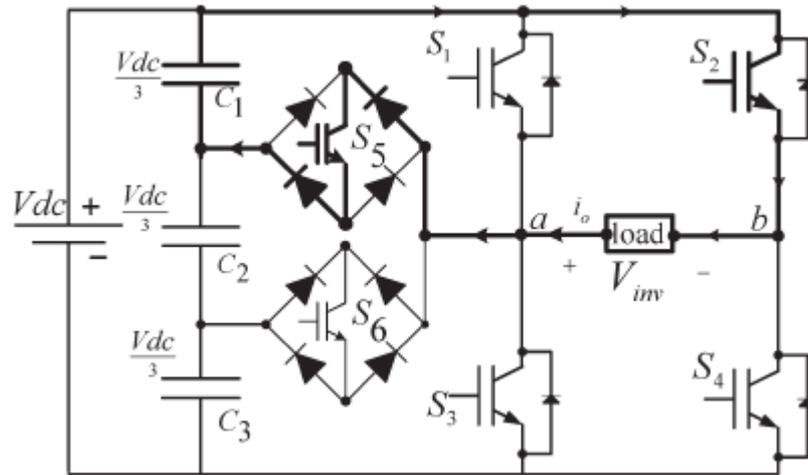


Fig: 2 (e) Switching combinations required to generate the output voltage $V_{ab} = v_{dc}/3$

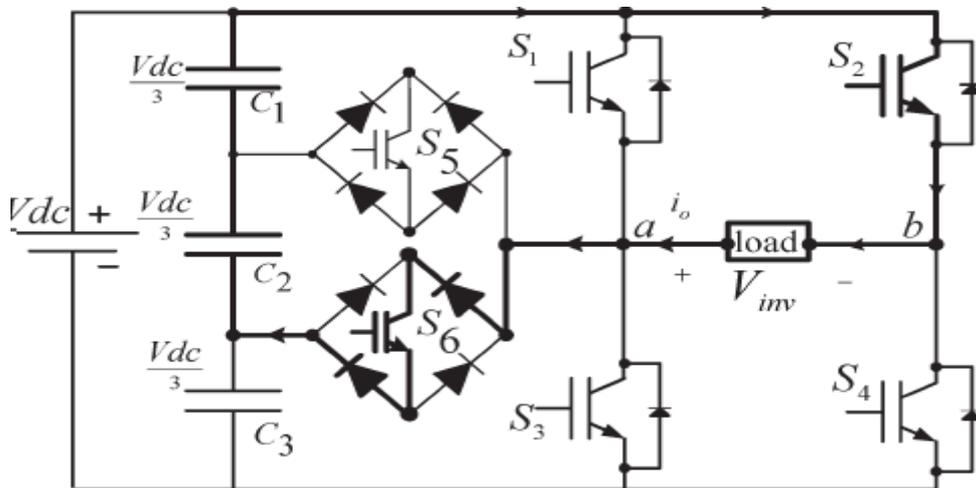


Fig: 2 (f) Switching combinations required to generate the output voltage $V_{ab} = -2v_{dc}/3$

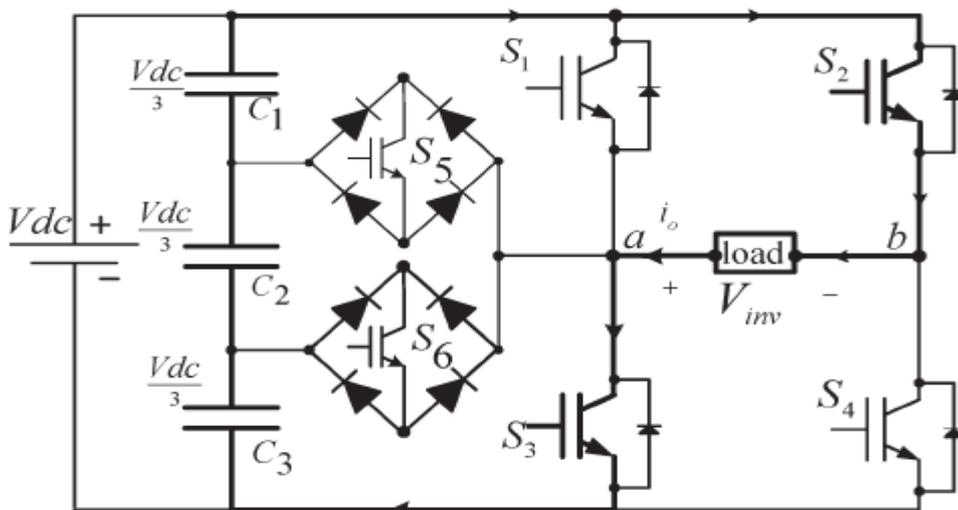


Fig: 2 (g) Switching combinations required to generate the output voltage $V_{ab} = -v_{dc}$

Two-third negative output ($-2V_{dc}/3$): The bidirectional switch S_6 is ON, connecting the load positive terminal, and S_2 is ON, connecting the load negative terminal to ground. All other controlled switches are OFF; the voltage applied to the load terminals is $-2V_{dc}/3$. Fig. 2(f) shows the current paths that are active at this stage

Maximum negative output ($-V_{dc}$): S_2 is ON, connecting the load negative terminal to V_{dc} , and S_3 is ON, connecting the load positive terminal to ground. All other controlled switches are OFF; the voltage applied to the load terminals is $-V_{dc}$. Fig. 2(g) shows the current paths that are active at this stage

TABLE-1: Output Voltage according to the Switches On-Off Condition

V_0	S_1	S_2	S_3	S_4	S_5	S_6
V_{dc}	ON	OFF	OFF	ON	OFF	OFF
$2V_{dc}/3$	OFF	OFF	OFF	ON	ON	OFF
$V_{dc}/3$	OFF	OFF	OFF	ON	OFF	ON
0	OFF	OFF	ON	ON	OFF	OFF
0*	ON	ON	OFF	OFF	OFF	OFF
$-V_{dc}/3$	OFF	ON	OFF	OFF	ON	OFF
$-2V_{dc}/3$	OFF	ON	OFF	OFF	OFF	ON
$-V_{dc}$	OFF	ON	ON	OFF	OFF	OFF

III. PWM MODULATION

A novel PWM modulation technique was introduced to generate the PWM switching signals. Three reference signals (V_{ref1} , V_{ref2} , and V_{ref3}) were compared with a carrier signal ($V_{carrier}$). The reference signals had the same frequency and amplitude and were in phase with an offset value that was equivalent to the amplitude of the carrier signal. The reference signals were each compared with the carrier signal. If V_{ref1} had exceeded the peak amplitude of $V_{carrier}$, V_{ref2} was compared with $V_{carrier}$ until it had exceeded the peak amplitude of $V_{carrier}$. Then, onward, V_{ref3} would take charge and would be compared with $V_{carrier}$ until it reached zero. Once V_{ref3} had reached zero, V_{ref2} would be compared until it reached zero. Switches S_1 , S_3 , S_5 , and S_6 would be switching at the rate of the carrier signal frequency, whereas S_2 and S_4 would operate at a frequency that was equivalent to the fundamental frequency. For one cycle of the fundamental frequency, the proposed inverter operated through six modes. The six mode operations are the described as follows
 Mode 1 : $0 < \omega t < \vartheta_1$ and $\vartheta_4 < \omega t < \pi$
 Mode 2 : $\vartheta_1 < \omega t < \vartheta_2$ and $\vartheta_3 < \omega t < \vartheta_4$
 Mode 3 : $\vartheta_2 < \omega t < \vartheta_3$
 Mode 4 : $\pi < \omega t < \vartheta_5$ and $\vartheta_8 < \omega t < 2\pi$
 Mode 5 : $\vartheta_5 < \omega t < \vartheta_6$ and $\vartheta_7 < \omega t < \vartheta_8$
 Mode 6 : $\vartheta_6 < \omega t < \vartheta_7$.

The phase angle depends on modulation index M_a . Theoretically, for a single reference signal and a single carrier signal, the modulation index is defined to be

$$M_a = \frac{A_m}{A_c} \text{-----}2$$

while for a single-reference signal and a dual carrier signal, the modulation index is defined to be

$$M_a = A_m/2A_c \text{-----}3$$

Since the proposed seven-level PWM inverter utilizes three carrier signals, the modulation index is defined to be

$$M_a = A_m/3A_c \text{-----}4$$

where A_c is the peak-to-peak value of the carrier signal and A_m is the peak value of the voltage reference signal V_{ref} . When the modulation index is less than 0.33, the phase angle displacement is

$$\theta_1 = \theta_2 = \theta_3 = \theta_4 = \frac{\pi}{2} \text{-----}5$$

$$\theta_5 = \theta_6 = \theta_7 = \theta_8 = 3\frac{\pi}{2} \text{-----}6$$

On the other hand, when the modulation index is more than 0.33 and less than 0.66, the phase angle displacement is determined by

$$\theta_1 = \sin^{-1} ab \text{-----}7$$

$$\theta_2 = \theta_3 = \frac{\pi}{2} \text{-----}8$$

$$\theta_4 = \pi - \theta_1 \text{-----}9$$

$$\theta_5 = \pi + \theta_1 \text{-----}10$$

$$\theta_6 = \theta_7 = 3\pi/2 \text{-----}11$$

$$\theta_8 = 2\pi - \theta_1 \text{-----}12$$

If the modulation index is more than 0.66, the phase angle displacement is determined by

$$\theta_1 = \sin^{-1} A c \frac{ac}{am} \text{-----}13$$

$$\theta_2 = (\sin^{-1} AC/Am |AC) \text{-----}14$$

$$\theta_3 = \pi - \theta_2 \text{-----}15$$

$$\theta_4 = \pi - \theta_1 \text{-----}16$$

$$\theta_5 = \pi + \theta_1 \text{-----}17$$

$$\theta_6 = \pi + \theta_2 \text{-----}18$$

$$\theta_7 = 2\pi - \theta_2 \text{-----}19$$

$$\theta_8 = 2\pi - \theta_1 \text{-----}20$$

For Ma that is equal to, or less than, 0.33, only the lower reference wave (V_{ref3}) is compared with the triangular carrier signal. The inverter's behavior is similar to that of a conventional full-bridge three-level PWM inverter. However, if Ma is more than 0.33 and less than 0.66, only V_{ref2} and V_{ref3} reference signals are compared with the triangular carrier wave. The output voltage consists of five dc-voltage levels. The modulation index is set to be more than 0.66 for seven levels of output voltage to be produced. Three reference signals have to be compared with the triangular carrier signal to produce switching signals for the switches.

IV. CONTROL SYSTEM

As Fig. 3 shows, the control system comprises a MPPT algorithm, a dc-bus voltage controller, reference-current generation, and a current controller. The two main tasks of the control system are maximization of the energy transferred from the PV arrays to the grid, and generation of a sinusoidal current with minimum harmonic distortion, also under the presence of grid voltage harmonics. If the power was increasing, the perturbation would continue in the same direction in the next cycle; otherwise, the direction would be

reversed. This means that the array terminal voltage is perturbed every MPPT cycle; therefore, when the MPP is reached, the P&O algorithm will oscillate around it. The P&O algorithm was implemented in the dc-dc boost converter. The output of the MPPT is the duty-cycle function. As the dc-link voltage V_{dc} was controlled in the dc-ac seven level PWM inverter, the change of the duty cycle changes the voltage at the output of the PV panels. A PID controller was implemented to keep the output voltage of the dc-dc boost converter (V_{dc}) constant by comparing V_{dc} and V_{dc} ref and feeding the error into the PID controller, which subsequently tries to reduce the error. In this way, the V_{dc} can be maintained at a constant value and at more than 2 of V_{grid} to inject power into the grid. To deliver energy to the grid, the frequency and phase of the PV inverter must equal those of the grid; therefore, a grid Synchronization method is needed.

The proposed inverter provides an analog zero-crossing detection circuit on one of its input ports where the grid voltage is to be connected. The zero-crossing circuit then produces an in-phase square-wave output that is fed into the digital I/O port on eZdsp board TMS320F2812. A PI algorithm was used as the feedback current controller for the application. The current injected into the grid, also known as grid current I_{grid} , was sensed and fed back to a comparator that compared it with the reference current $I_{gridref}$. $I_{gridref}$ is the result of the MPPT algorithm. The error from the comparison process of I_{grid} and $I_{gridref}$ was fed into the PI controller. The output of the PI controller, also known as V_{ref} , goes through an anti windup process before being compared with the triangular wave to produce the switching signals for S1-S6. Eventually, V_{ref} becomes V_{ref1} ; V_{ref2} and V_{ref3} can be derived from V_{ref1} by shifting the offset value, which was equivalent to the amplitude of the triangular wave.

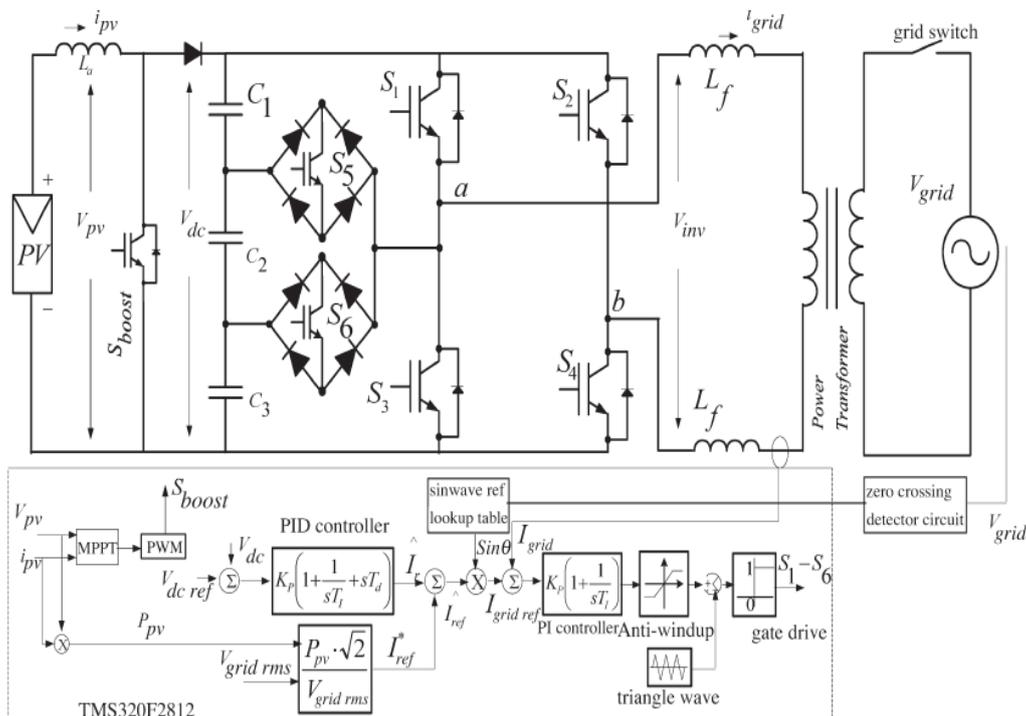


Fig:3 Seven level inverter with Closed loop Control Algorithm

V.SIMULATION RESULTS

MATLAB SIMULINK simulated the proposed configuration before it was physically implemented in a prototype. The PWM switching patterns were generated by comparing three reference signals (V_{ref1} , V_{ref2} , and V_{ref3}) against a triangular carrier signal. Subsequently, the comparing process produced PWM switching signals for switches S_1 – S_6 . Therefore, operation is recommended to be between $Ma = 0.66$ and $Ma = 1.0$. V_{inv} comprises seven voltage levels, namely, V_{dc} , $2V_{dc}/3$, $V_{dc}/3$, 0 , $-V_{dc}$, $-2V_{dc}/3$, and $-V_{dc}/3$. The current flowing into the grid was filtered to resemble a pure sine wave in phase with the grid voltage (see As I_{grid} is almost a pure sine wave at unity power factor, the total harmonic distortion (THD) can be reduced compared with the THD. Comparing all three THD measurements, the seven-level inverter produced the lowest THD compared with the five- and three-level ones. This proves that, as the level increases, the THD reduces, which is an essential criterion for grid-connected PV systems.

Fig 4 shows the matlab circuit diagram for the without pwm technique circuit . Fig 5 shows the without output voltages for the without pwm technique circuit in this out put voltage the pulse modulating switches can not applied in this circuit PWM modulation technique was introduced to generate the PWM switching signals. Three reference signals (V_{ref1} , V_{ref2} , and V_{ref3}) were compared with a carrier signal ($V_{carrier}$). The reference signals had the same frequency and amplitude and were in phase with an offset value that was equivalent to the amplitude of the carrier signal. The reference signals were each compared with the carrier signal. If V_{ref1} had exceeded the peak amplitude of $V_{carrier}$, V_{ref2} was compared with $V_{carrier}$ until it had exceeded the peak amplitude of $V_{carrier}$. Then, onward, V_{ref3} would take charge and would be compared with $V_{carrier}$ until it reached zero. Once V_{ref3} had reached zero, V_{ref2} would be compared until it reached zero. Then, onward, V_{ref1} would be compared with $v_{carrier}$

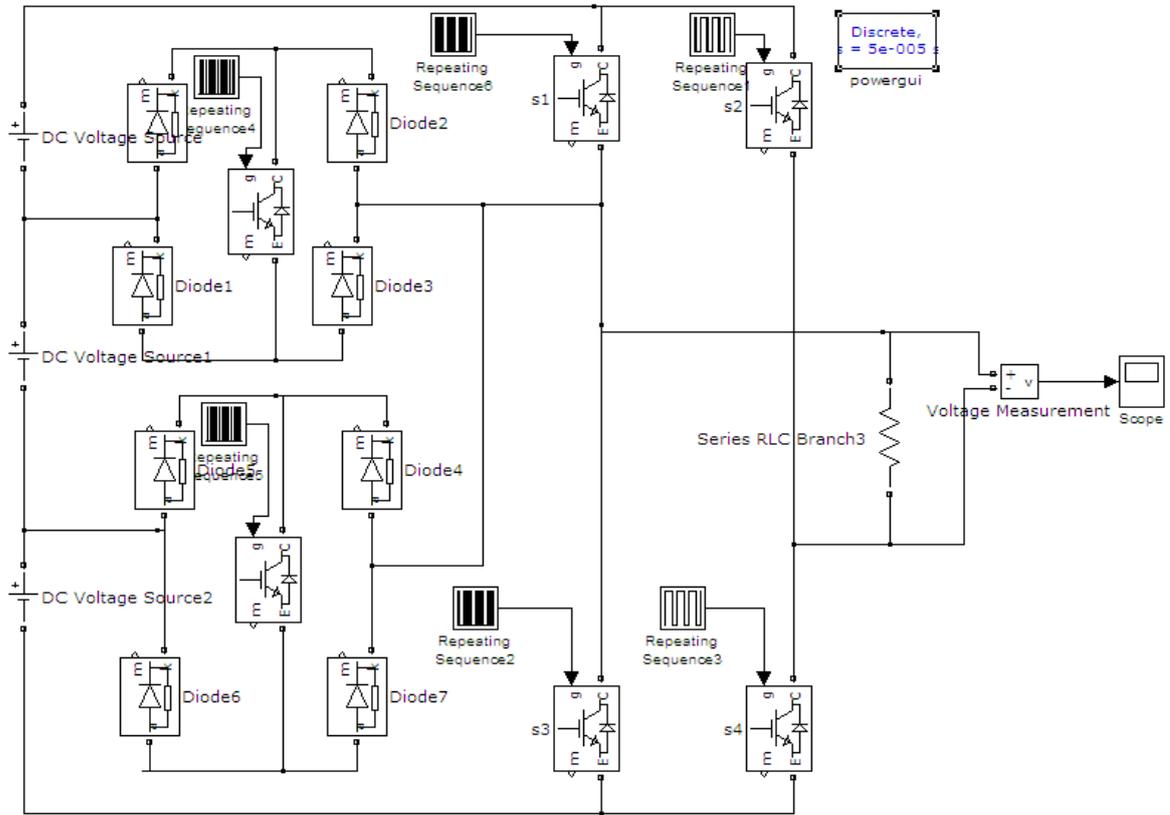


Fig:4 Without PWM Technique Circuit

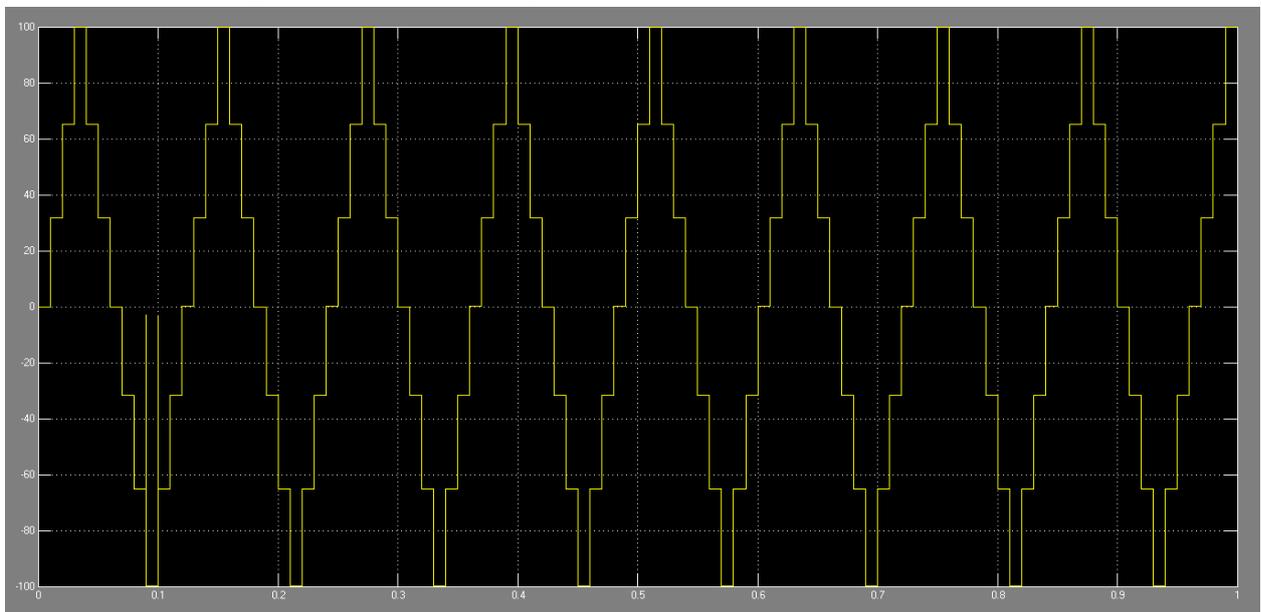


Fig:5 without PWM technique Circuit

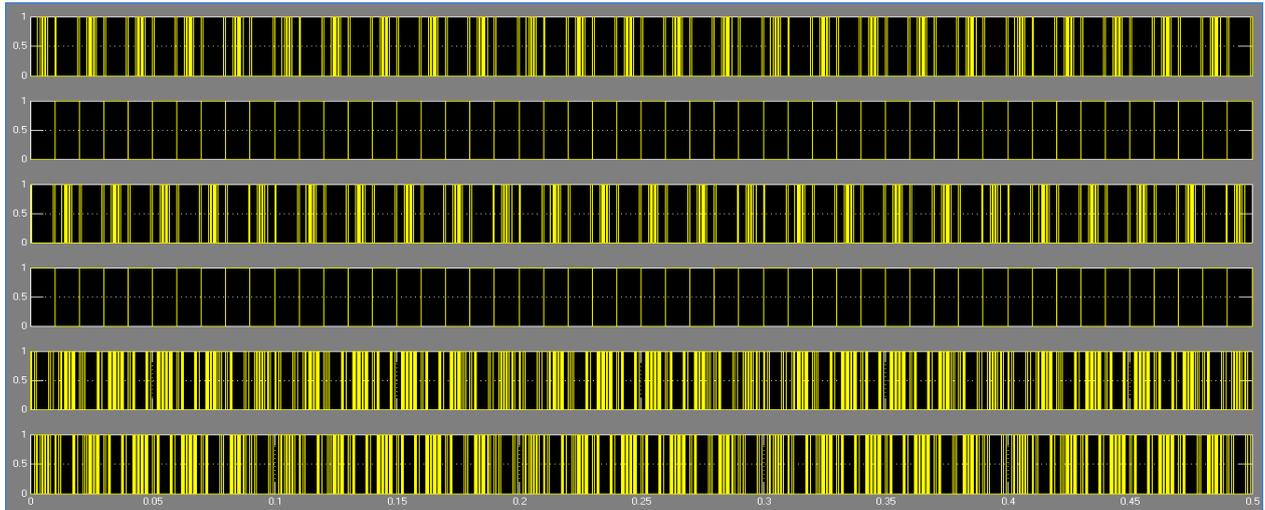


Fig:6 PWM Switching Pulses

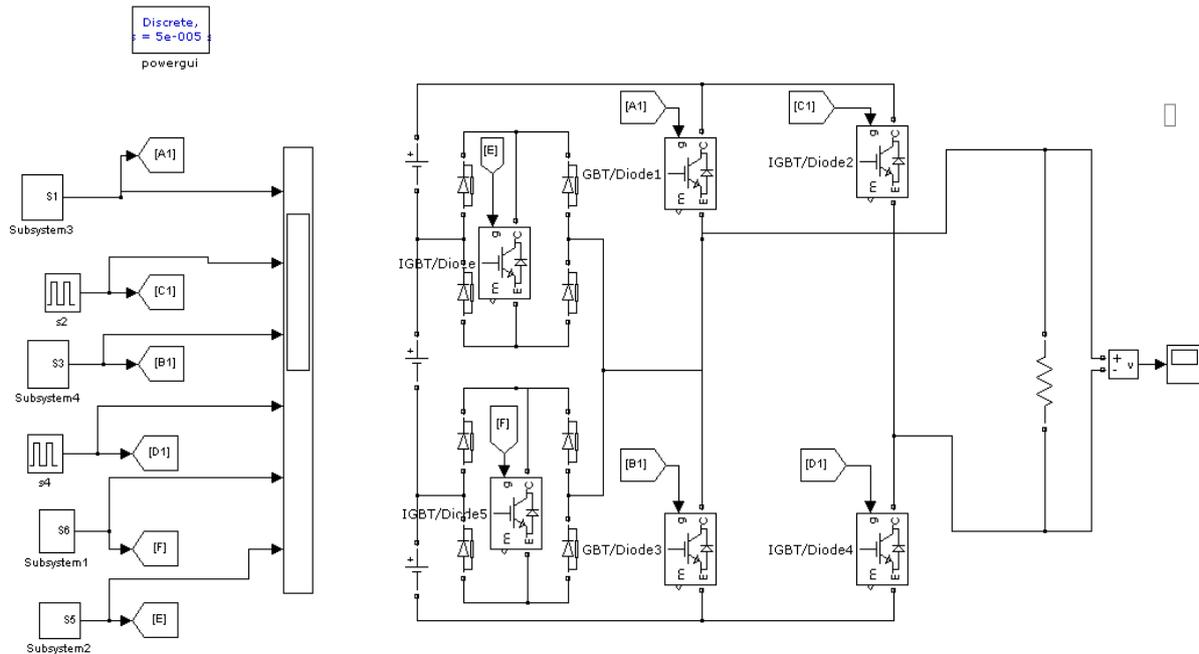


Fig:7 With PWM Technique Circuit

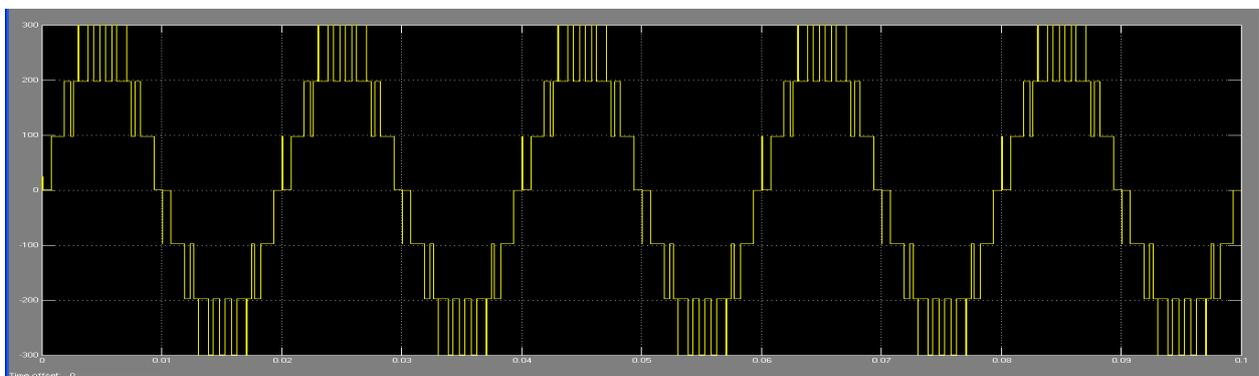


Fig:8 Out put voltages with PWM technique

Fig. 7 shows the Matlab/ Simulink model of grid connected photovoltaic system. It consist of a DC to DC conversion stage and Dc to AC multilevel inversion stage. Fig. 8 shows the seven level PWM output. Fig. 8 shows the grid voltage and grid current. From the figure it is clear that grid voltage and current are in pahse. Fig. 8 shows the output of proposed nine level inverter. In proposed converter for nine level seven switches are required. In order to produce the same levels cascaded H-Bridge requires sixteen switches.

CONCLUSION

Multilevel inverters offer improved output waveforms and lower THD scheme for the proposed. It utilizes three reference signals and a triangular carrier signal to generate PWM switching signals.. By controlling the modulation index, the desired number of levels of the inverter's output voltage can be achieved. A TMS320F2812 DSP optimized the performance of the inverter. The less THD in the seven-level inverter compared with that in the five- and three-level inverters is an attractive solution for grid-connected PV inverters.

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